MODEL 8730

TIME CODE READER

OPERATING AND SERVICE MANUAL

SERIAL NO. C001

AUSTRON

AUSTRON INC. P.O. BOX 14766 - EXIT 248, N. IH 35, AUSTIN, TEXAS 78761 (512) 251-2341 TWX 910/874-1356

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OPERATING AND SERVICE MANUAL

SERIAL NO. C001

DECEMBER 1985

P/N 12708720

REVISION B

WARRANTY

AUSTRON, Inc. of Austin, Texas, warrants for one year after delivery to the original purchaser of any product manufactured by AUSTRON, that same shall be free of defects in material and workmanship. Obligation under this warranty shall be limited to repair or replacement, at AUSTRON's discretion, of any product or part thereof which has been returned by the original purchaser with transportation prepaid, and upon examination by AUSTRON, is found to be defective. AUSTRON assumes no responsibility for loss or damage to equipment being returned for repair or replacement under the terms of this warranty.

For this warranty to be effective, the purchaser agrees that the equipment will be properly installed and maintained. Equipment which, upon examination by AUSTRON, requires repair or replacement of parts thereof as a result of improper installation, misuse, unauthorized alterations or repairs, or user negligence, such repairs or replacement of parts thereof will be made at cost.

AUSTRON makes no representation or warranty of any kind, either expressed or implied, with respect to equipment operation and procedures. Any action that the user may take in reliance upon the operation or accuracy of this equipment shall be taken solely upon the user's own responsibility and risk.

AUSTRON shall not be liable for consequential damages to purchaser, user, or any others resulting from the possession or use of this equipment.

Prior to return of a product under terms of this warranty, AUSTRON, Inc., Austin, Texas, is to be notified. Notification is to include the model number and serial number of the product and full details of the problem.

MODEL 8730 TIME CODE READER

INTRODUCTION

This manual is for personnel operating or maintaining the Model 8730 Time Code Reader manufactured by AUSTRON, Inc. It contains information concerning the physical and electrical specifications, installation, adjustment and operational procedures, and theoretical descriptions. In addition, the manual provides parts lists, assembly drawings, schematics and block diagrams.

AMENDMENT NOTICE

AUSTRON, Inc. makes every attempt to provide up-to-date manuals with the associated equipment. Occasionally, changes are made to the equipment wherein it is necessary to provide amendments to the manual. If any amendments are provided for this manual they are printed on paper stock other than white and will be found at the rear of this manual.

NOTE

The content of any amendments may affect operation, maintenance or calibration of the equipment.

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1. GENERAL DESCRIPTION

1.1. SCOPE OF SECTION

Section One introduces the AUSTRON Model 8730 Time Code Reader. Provided here is the description of the equipment including variations and options. Also, there is a brief discussion of the Model 8730's input and output signals as well as environment and power requirements.

1.2. PURPOSE OF EQUIPMENT

The Model 8730 Time Code Reader accepts a serial BCD time code on an amplitude modulated carrier and translates it into parallel form for display and optional external use. The display and optional parallel BCD outputs are in days, hours, minutes and seconds. The direction of the incoming code is sensed automatically within the unit. Translated time is on-time in the forward direction.

The unit is completely self-contained, requiring only the serial input code and a source of 115/230 Vac, 48 Hz to 440 Hz or 12 Vdc power. CMOS circuitry is used throughout for its low power requirements and high noise immunity.

1.3. MODEL VARIATIONS

Any one of several input code formats can be accommodated in the Model 8730 by changing code option PCBs and/or a rear panel switch position. Common code formats include: NASA 36-bit, switch-selectable IRIG A/B and switch-selectable XR3 250 Hz/1 kHz. These standard options are described in Section Six when included with the unit. Other options include parallel BCD outputs and coincidence outputs at a preselected time.

Table. 1-1: Model 8730 Available Options.

Option	Description
A17	Coincidence output at preset time in days, hours, minutes and seconds
C18	NASA 36-Bit Time Code
C41	IRIG A/B Time Code, switch-selectable
C47	XR3 (250 Hz/1 kHz) Time Code, switch-selectable
D15	Parallel BCD Output, days, hours, minutes and seconds

1.4. SPECIFICATIONS

1.4.1. Display

The Model 8730 has a nine digit, seven segment, high efficiency LED display to indicate time in days, hours, minutes and seconds. The numerals are 0.43 inch (11 mm) high and are red in color. Lighted colons are provided between days, hours, minutes and seconds.

1.4.2. Code Format

The Model 8730 code format is determined by the choice of plug-in options. NASA 36, IRIG A/B (switch-selectable), and XR3 250 Hz/1 kHz (switch-selectable) are the options available. Sensing of forward or reverse direction of code is automatic.

1.4.3. Input Modulated Code

The carrier frequency may vary from 50 Hz to 250 kHz with modulation ratios from 2:1 to 6:1. The input level may vary from 100 mV to 10 Vp-p. The input impedance is greater than 100 kilohms. The input code passes through a rear panel BNC, J2.

1.4.4. Outputs

All outputs are buffered, positive level, positive true, DTL/TTL compatible signals supplied via a rear panel 50-pin connector, Amphenol 57-40500. A mating 50-pin connector (57-30500) is supplied.

ONE = 5 Vdc $\pm$0.5 Vdc @ 1.2 mA

ZERO = 0 $\pm$0.1 Vdc, 3.2 mA sink

1.4.4.1. Level Shift (DC) Code Output

The Model 8730 provides a dc-level shift version of the input code at rear panel connector, (J1, 47).

1.4.4.2. Inhibit Read Output

At update time in the forward Read mode, the inhibit read pulse is high during propagation of update information through the accumulator. It is used with optional parallel BCD outputs. (Connector pin 46.)

1.4.4.3. Pulse Rate Outputs

1 pps and carrier frequency pulse rates go positive on-time. The 1 pps rate has a 10 percent duty cycle and the carrier 50 percent. (Connector pins 20 and 45, respectively.)

1.4.5. Environmental Requirements

The unit operates normally from 0°C (32°F) to 50°C (122°F) in up to 95 percent relative humidity.

The storage temperature is 85°C (185°F) maximum and -55°C (-69°F) minimum.

1.4.6. Power Requirements

The Model 8730 takes 115 Vac or 230 Vac ±10 percent, 48 Hz to 440 Hz, via a rear panel three-pin connector, J101, (power cable supplied) or 12 Vdc ±3 Vdc via a rear panel terminal board. Power required is less than 4 watts. AC and dc power may be connected simultaneously, the ac input dominates. The unit is supplied from the factory for 115 Vac operation. Conversion to 230 Vac is by internal jumper change. Refer to Section Two for installation.

1.4.7. Physical Requirements

Size

The unit is 1.75 in (4.4 cm) high by 9.5 in (24.1 cm) wide by 12 in (30.4 cm) deep.

Weight

The unit weighs less than 8 lbs (3.6 kg).

2. INSTALLATION

2.1. SCOPE OF SECTION

Section Two describes the steps required to prepare the Model 8730 Time Code Reader for operation and reshipment to another location. Included in this section are instructions for unpacking, inspecting, installing and storing the unit.

2.2. UNPACKING AND INSPECTION

Upon receipt of the unit, verify that it is intact and as ordered. Inspect the instrument for any damage. If shipping damage is found, refer to the warranty in the front of this manual, and to Section 2.4 for general packaging instructions.

2.3. INSTALLING THE UNIT

As soon as possible, install the instrument and thoroughly inspect to ensure compliance with the specifications cited in Section 1.4. Should the instrument fail to meet specifications, immediately contact your AUSTRON representative.

The following paragraphs describe installation procedures including power hook-ups and cabling requirements for installation.

2.3.1. Rear Panel Controls and Connectors

Rear panel controls and connectors are listed in Table 2-1.

Table. 2-1: Rear Panel Controls and Connectors.

	Device	Function
1.	BCD/PULSE RATE (50-pin connector, J1)	Pulse Rate, DC Code and Inhibit Read (Computer Read Command) outputs plus optional coincidence and/or parallel BCD days, hours, minutes and seconds
2.	CODE IN (BNC, J2)	Time Code input
3.	115/230 Vac (receptacle with line filter, J101)	Mates with line cord to 115 Vac to 230 Vac, 48 Hz to 440 Hz power source. (230 Vac operation requires internal jumper change, see Section Two.)
4.	12 Vdc (TB1)	Accepts 12 Vdc ±3 Vdc power input
5.	IRIG A/B or XR3 250 Hz/1 kHz (slide switch, A3S1)	Code selector, switch accessible through rear panel when IRIG A/B (Option C41) or XR3 250 Hz /1 kHz (Option C47) is installed
6.	F1 1/8 A Slo Blo (fuse holder)	AC power fuse

2.3.2. Power Hook-Up and Jumper Connections

The Model 8730, unless otherwise specified, is supplied to operate from 9 Vdc to 15 Vdc or 115 Vac/230 Vac ±10%, 48 Hz to 440 Hz. Either dc or ac or both may be connected to the unit. If both are connected, the unit will take power from the ac source.

To modify the unit to operate from 230 Vac ±10%, 48 Hz to 440 Hz, refer to Figure 2-1 and proceed with the following steps:

1. Remove the top and bottom covers.
2. Unsolder and remove jumpers W1 and W2.
3. Add jumper W3.
4. If necessary, circuit and chassis grounds are separated by removing jumper W4.

2.4. STORAGE AND RESHIPMENT

Ensure the environmental conditions during storage and reshipment are limited as follows:

Maximum Temperature: 185°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the original factory packaging, or use the best packaging methods available. Contract packing companies can provide dependable packaging on short notice.

General packaging instructions:

1. Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

2. If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb/sq in bursting strength) or wooden box to house the instrument.

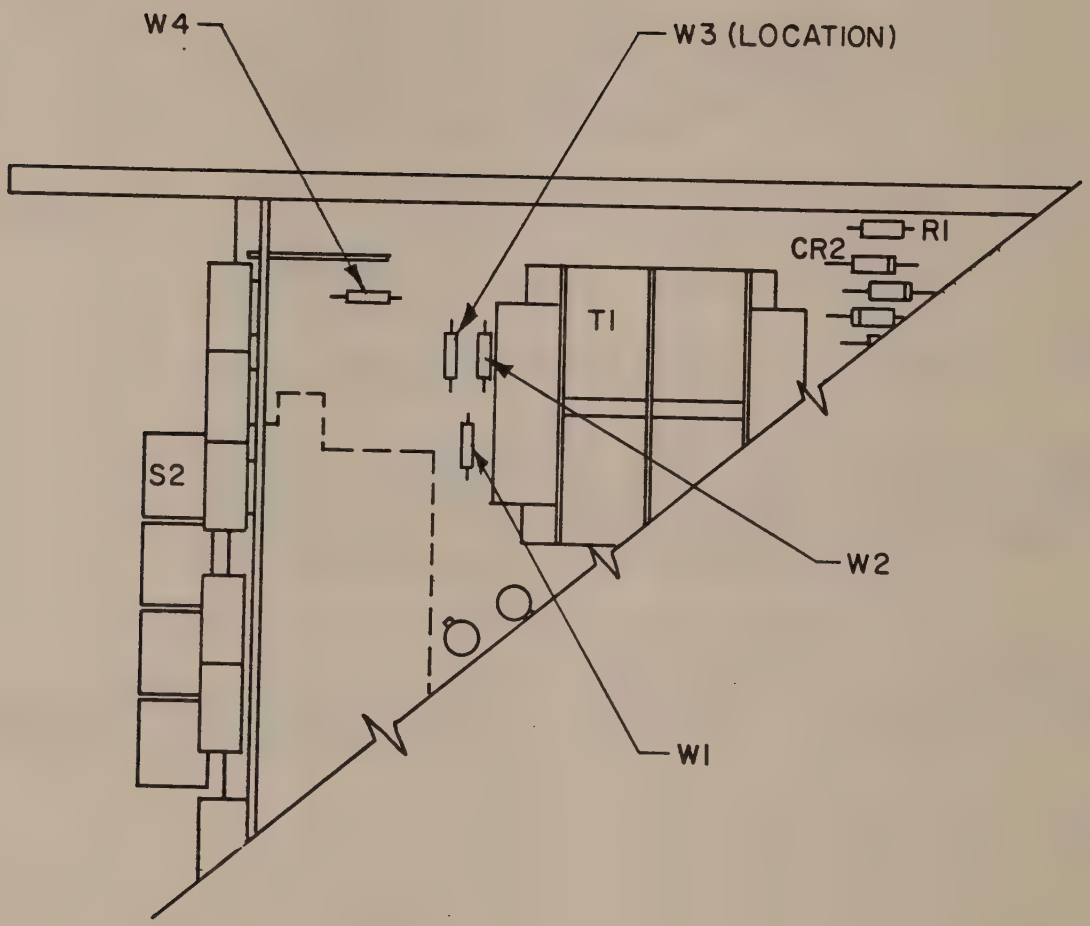
3. Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

4. Seal the package with strong tape or metal bands. Mark container with "DELICATE INSTRUMENT".

5. If returning the unit to AUSTRON, refer to the warranty in the front of this manual and check with your AUSTRON representative for instructions before shipping.

Refer to the instrument by model number and full serial number in all correspondence.

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
—	RELEASED	11.19.85	OK



		TOLERANCES UNLESS OTHERWISE SPECIFIED			AUSTRON INC. AUSTIN, TEXAS		
		DEC —	FRAC —	ANG —			
		MATERIAL: —			JUMPER LOCATION		
	Fig. 2-1						
—	8730	Q.A.			SIZE 1	CODE IDENT NO. 24672	12408830 REV —
EXT ASSY	USED ON	ENGR					
APPLICATION		CHECK					
		DRAWN	P. JOHNSON	11/19/85	SCALE NONE		SHEET | OF |

Initial Checkout

Initial checkout is accomplished after receipt of the instrument as part of the initial inspection. No initial adjustments are required.

NOTE

Internal adjustments located on the AGC & Cycle Detector module are set at the factory. See Section Four for the adjustment procedure.

The following checks detect any major internal shipping damage.

1. Connect the instrument to an appropriate ac or dc power source.

2. Place the power switch in the ON position. The display illuminates.

3. Connect an appropriate time code source to CODE IN, J2. Ensure this time code is within the amplitude ratio and frequency limits specified in Section One. The display updates with a forward code and downdates with a reverse code.

4. Check dc code and pulse rate outputs.

The unit is supplied for bench-top or tilt-stand operation. If panel mounting is required, an optional rack mounting kit is necessary.

3. OPERATION

3.1. SCOPE OF SECTION

Section Three details controls, indicators and connectors as to the operation of the Model 8730. Read the following description on use of the instrument controls, indicators and connectors before operating the unit.

The Model 8730 is a fully automatic instrument. No preliminary adjustments are required. The only operator controls provided are the power, error bypass and code format switches.

Refer to the specifications in Section One for operating temperature range and input signal characteristics.

3.2. CONTROLS, INDICATORS AND CONNECTORS

Front panel controls and indicators are described in Table 3-1.

Table. 3-1: Front Panel Controls and Indicators.

	Device	Function
1.	POWER ON/OFF (toggle switch S1)	Applies ac and/or dc power to the instrument
2.	ERROR BYPASS (ganged, 4-station push button switch S2)	Selects zero, two, four or eight frames of error bypass. Zero error bypass allows time information stripped from the input code to be loaded directly into the accumulator. Two, four or eight frames of error bypass inhibit transfer of input time data until after two, four or eight consecutive error frames are detected
3.	ERROR (LED indicator DS1)	Indicates a discrepancy between the input code and the contents of the accumulator
4.	DISPLAY	A nine-digit, in-line, in-plane, seven segment LED readout which indicates time in days, hours, minutes and seconds

3.3. POWER-UP PROCEDURE

To bring the unit to a fully operational condition, perform the following steps:

1. Verify POWER ON/OFF switch on the front panel is set to OFF.

2. Install the power cord and input signal cable.

3. Set the POWER ON/OFF to ON.

4. MAINTENANCE AND CALIBRATION

4.1. SCOPE OF SECTION

Section Four covers recommended maintenance and repair test equipment and procedures for the Model 8730. Also included are instructions for calibration of the time code reader.

4.2. FACTORY SERVICE

When your Model 8730 requires service that cannot be accomplished on site, contact your AUSTRON representative. He can provide field service or arrange for factory returns, when necessary. Address all inquiries on operation or applications to your sales representative:

AUSTRON, Inc.
P. O. Box 14766
Austin, TX 78761

Specify both model and complete serial number in all correspondence. If necessary, you may phone AUSTRON at (Area Code 512) 251-2341.

4.3. ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1. Disconnect power and remove the cover.

2. Make a thorough visual inspection of all wiring and cables. Check for frayed, loose or burned wires.

3. Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds and general physical damage. When a PCB contains integrated-circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4. Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

5. If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low-pressure stream of air to remove the foreign material.

CAUTION

Do not clean the PCB or small internal components with a stiff brush or solvents, since damage to the circuits may result. Do not use a high-powered vacuum cleaner device on small internal components.

6. Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints and other foreign materials.

7. Replace the cover and reconnect power. Perform the Operational Test and Calibration Procedure (Section 4.5). If performance does not match or exceed the specifications listed in Section One of this manual, corrective maintenance is in order.

4.4. PCB REPAIR RECOMMENDATIONS

When replacing integrated circuits or other electronic components soldered to PCBs, the procedures indicated below must be followed or damage to the board may result:

1. Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2. Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component.)

3. Apply heat (40-50 W soldering iron) sparingly to each of the cut pins or leads and remove from the board; clean the hole(s) with a toothpick or solder suction tool.

4. Form the leads of the replacement part and insert in the printed circuit holes; solder, then trim leads to extend 1/16 inch beyond the back surface of the board. (Use only 63-67 solder with maximum 1/16 inch diameter.)

CAUTION

Only trim semiconductor leads after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.

5. When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the soldered connection to cool before removing the heat sink.

6. Clean all dirt and solder-flux from the printed circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

4.5. OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction, the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the technician to isolate the trouble to a particular circuit board or subsection. When the trouble is isolated, the functional description in Section Five and option information in Section Six will facilitate repair.

4.5.1. Recommended Test Equipment

The following test equipment or equivalent in Table 4-1 is recommended for use in servicing the Model 8730.

Table. 4-1: Test Equipment for Model 8730.

Model	Manufacturer	Minimum Specifications
422	Tektronix, Inc.	Oscilloscope, 15 MHz bandwidth, triggered sweeps from 0.1 ms/cm to 5 s/cm. Vertical sensitivity from .05 V/cm to 20 V/cm
6012	Tektronix, Inc.	Probe, 10:1 attenuation ratio, 17 pF capacitance
7004A	Systron-Donner	DMM 10 Megohm input impedance, ±0.1 percent accuracy

In addition to the equipment listed above, a suitable source of input signals with known characteristics is required. This may be a time code generator or a prerecorded tape and tape playback equipment.

4.5.2. Power Supply
(Schematic Dwgs. 12307900-02 and 12307889-01)

The voltages listed below are necessary for proper operation of the unit. Check for the designated nominal levels at the indicated test points.

1. Regulated 8 Vdc at the junction of R49 and C2.

2. Regulated 8 Vdc (Vdd) at the junction of R49 and C5.

3. Regulated 5 Vdc (Vcc) at the junction of R50 and C6.

4.5.3. Each Cycle Adjustment
(Schematic Dwg. No. 12307878-01)

To adjust the Each Cycle (EC) Detector, perform the following steps:

1. Power up the unit.

2. Supply an input signal with the proper format, an amplitude of 3 Vp-p, to CODE IN, J2.

3. Adjust EC LEVEL potentiometer, R40, and EC HYST potentiometer, R42, for symmetrical square wave at (J1, 45).

5. FUNCTIONAL DESCRIPTION

5.1. SCOPE OF SECTION

Section Five includes detailed explanations of the Model 8730 circuit functions, with assembly drawings, logic and schematic diagrams, and parts lists for each circuit of the basic unit. Also included is a basic unit block diagram Dwg. No. 12307900-02.

The Model 8730 Time Code Reader must be equipped with one of the optional Reader Logic PCBs to be operational. A Reader Logic PCB is inserted (electrically) between the AGC & Cycle Detector and the Main Board Circuits. Refer to Section Six for a description of the particular Reader Logic PCB installed in your unit.

When equipped with a Reader Logic PCB the Model 8730 accepts a serial time code on an amplitude-modulated carrier, conditions it, determines its direction, strips out the time information and loads it into an accumulator under control of an error bypass circuit. The accumulated time is available in parallel BCD form for optional output. It is serialized and fed to a display, an error bypass circuit and (optionally) to a coincidence circuit.

The basic circuitry is described in this section under the headings listed below.

1. AGC & Cycle Detector
2. Reader Logic
3. Time-of-Year Accumulator
4. Error Bypass
5. Display Control
6. Display
7. Power Supply

The optional features mentioned here in Section Five are described in detail in Section Six, when included in the unit.

NOTE

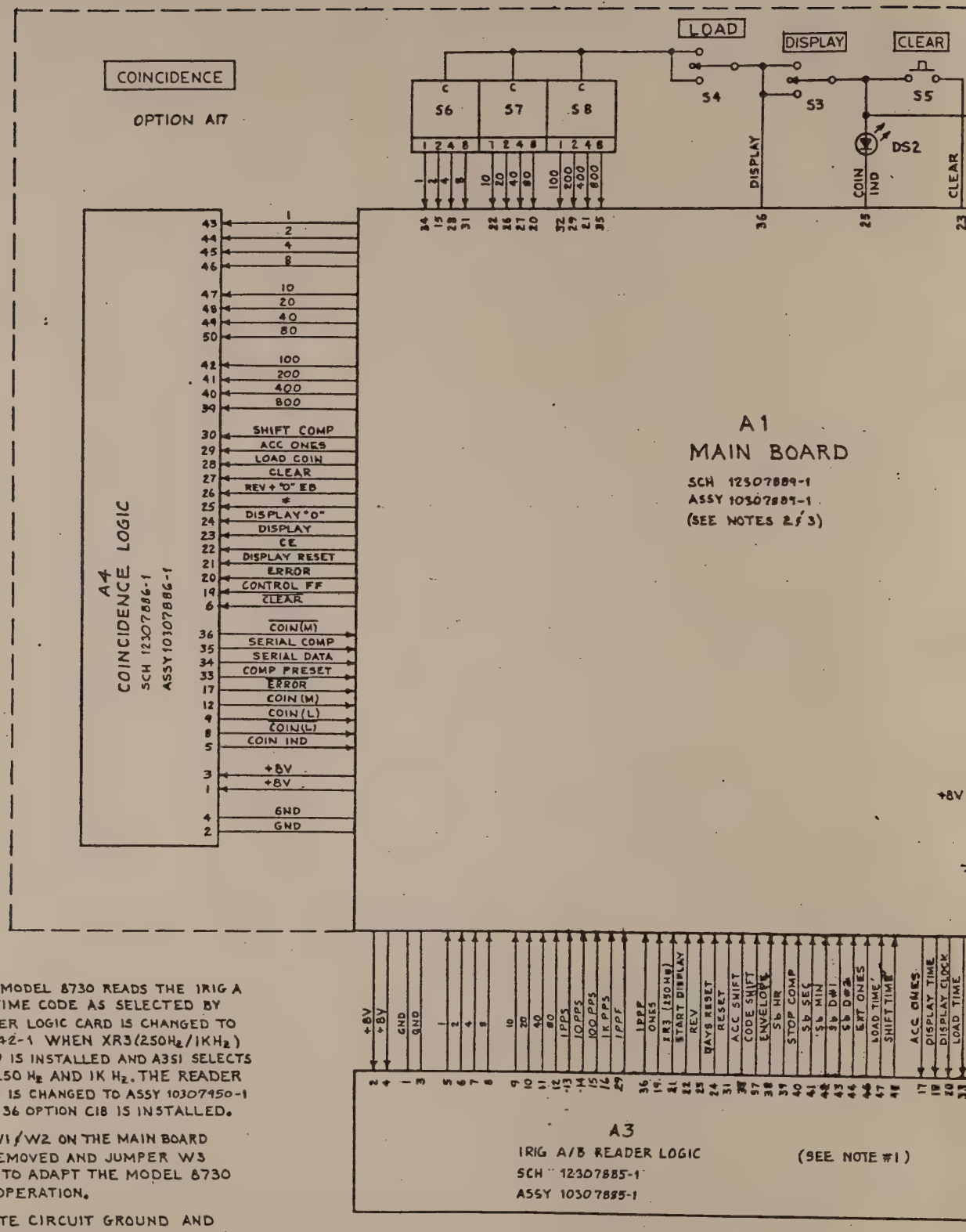
CMOS integrated circuits are used throughout the Model 8730. In general, these are Motorola B-Series devices which are described in detail in the Motorola CMOS Catalog (Volume 5/Series B). RCA equivalents for most of the devices may be found in the RCA COS/MOS Integrated Circuits Catalog (SSD-2-3C).

Reference Designators

The reference designators used in the Model 8730 are listed in Table 5-1.

Table. 5-1: Reference Designators.

Symbol	Component
A	Printed Circuit Board (PCB) or Module Assembly
C	Capacitor
CR	Diode
DS	Lamp
F	Fuse
J	Jack
L	Inductor
P	Plug
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TB	Terminal Board
TP	Test Point
U	Integrated Circuit
UR	Resistor Pack
VR	Voltage Regulator (Zener)
W	Jumper
X	Socket



NOTES:

1. THE BASIC MODEL 8730 READS THE IRIG A OR IRIG B TIME CODE AS SELECTED BY A3S1. READER LOGIC CARD IS CHANGED TO ASSY 10308142-1 WHEN XR3 (250 H_z / 1K H_z) OPTION C47 IS INSTALLED AND A3S1 SELECTS BETWEEN 250 H_z AND 1K H_z. THE READER LOGIC CARD IS CHANGED TO ASSY 10307950-1 WHEN NASA 36 OPTION C18 IS INSTALLED.
2. JUMPERS W1/W2 ON THE MAIN BOARD MUST BE REMOVED AND JUMPER W3 INSTALLED, TO ADAPT THE MODEL 8730 FOR 230V OPERATION.
3. TO SEPERATE CIRCUIT GROUND AND CHASSIS GROUND, REMOVE JUMPER W4 ON THE MAIN BOARD.

REV	DESCRIPTION	ENG. NO.	ECO NO.	DATE	APP. BY
A	RELEASED TO RECORDS		19418	7/24/81	
B	A1-42 WAS -40; A5 WAS 08119203		19418	7/24/81	K.MM.
B1	A1-42 WAS A1-38; A1-40 WAS A1-42.	—	NFC	7/13/81	RAS
C	DWG NO. WAS 07190002		9837		

ERROR

ERROR BYPASS 0 2 4 8 S2

DS1

VDD ERROR IND O'FLO 0 2 4 8 COM

13 14 10

ON

S1

OFF

F1 1/8A SB

J101 LINE FILTER

115/230V 48-440 Hz (SEE NOTE #2)

SEGMENT SELECT LINES a b c d e f g

DISPLAY P/O A1
SCH: 12307877-1
ASSY 10307877-1

6 8 4 3 10 5 9

1 16 13 17 VDD

20 19 18 15 14 12 11 7 2

DX10 DX10 DX1 HX10 HX1 MX10 MX1 SX10 SX1

DIGIT SELECT LINES

1S	1	
2S	2	
4S	26	
8S	27	
10S	3	
20S	4	
40S	28	
GND	29	
1M	5	
2M	6	
4M	30	
8M	31	
10M	7	
20M	8	
40M	32	
GND	33	
1H	9	
2H	10	
4H	34	
8H	35	
10H	11	
20H	12	
GND	36	
GND	37	
1D	13	
2D	14	
4D	38	
8D	39	
10D	15	
20D	16	
40D	40	
80D	41	
100D	17	
200D	18	
GND	42	
GND	43	
COIN (L)	19	
COIN (M)	44	
COIN CLEAR	21	
SPARE	22	
	23	
	24	
	25	
1 PPS	20	
CARRIER	45	
INHIBIT READ	46	
DC CODE	47	
GND	48	
GND	49	
CHASSIS GND	50	

PARALLEL BCD OUTPUTS (OPTION D15)

BCD/PULSE RATE

P/O COINCIDENCE OPTION A17

A1J1
AMPH # 57-40500
MATE: # 57-30500

A2
AGC & CYCLE DETECTOR
SCH 12307878-1
ASSY 10307878-1

GND

J2

CODE IN

ERROR LLC EC

35 49 50

A3 S1

A IRIG B 250 XR3 1K

SEE NOTE 1

41 19 39 12 40

1PPS 1KPPS Vcc +16 GND CHASSIS GND

SCH: 12308191-1
ASSY: 10308191-1
A5

MILLISECONDS OUTPUT E14 OPTION

3 4 5 6 7 8 11 12

COM

U101 7808

IN OUT

Q101 2N4918

TB1

+ 12 VDC

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN	LA 6-17-81 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	AUSTRON AUSTIN, TEXAS
CHECK	DATE		
ELECT.	DATE		
MECH	DATE		CODE IDENT. 24672
APPROVED	DATE		
QA	DATE		MATERIAL
SCALE	DO NOT SCALE DRAWING	SH 1 OF 1	

8730% | 1146+
USED ON | NEXT ASSY
APPLICATION

MODEL 8730 TIME CODE READER BLOCK DIAG

DRAWING NO.

REF	SIZE	PART NO.	REV
-	D	12307900-2	C

ASSEMBLY SHIPPING ASSY,8730
ASSEMBLY NUMBER 30608665-2
REFERENCE DESIGNATOR PREFIX
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
1	FINAL ASSY 8730	25607900-2		24672
1P1	CONN 50 PIN PLUG	551306-0050	57-30500	02660
1W1	POWER CORD	570076-0007	17500B	70903

ASSEMBLY FINAL ASSY 8730
ASSEMBLY NUMBER 25607900-2
REFERENCE DESIGNATOR PREFIX 1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	PANEL ASSY, FRONT 8730	10907897-2		24672
A2	PANEL ASSY, REAR 8730	10907862-2		24672
A3	CHASSIS CKT. ASSY 8730	20607899-2		24672
MP1	TILT STAND, HALF RACK BOX	01100716		24672
MP2	FOOT LEFT HND W/BAIL	520206-0011	PP40012-1	21604
MP3	FOOT RHT HND USE W/BAIL	520206-0012	PP40012-2	21604
MP4	FOOT REAR MOLD POLYPR	520206-0013	PP40013-1	21604
MP5	FOOT REAR MOLD POLYPR	520206-0013	PP40013-1	21604

ASSEMBLY PANEL ASSY,FRONT 8730
ASSEMBLY NUMBER 10907897-2
REFERENCE DESIGNATOR PREFIX 1A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
DS1	LED CLR DIFF .200 50 MA	555600-4887	HLMP-0240	28480
MP1	WINDOW	02007860		24672
S1	SW TOGGLE DPDT MIN ON-NONE-ON	553010-0050	7201SYZQ	09353
SIMP1	NUT DRESS 1/4-40 NICK/PLATE	401000-0000	87099	09353
XDS1	LAMP HOLDER	555001-0003	0-084-3D	03797

ASSEMBLY PANEL ASSY, REAR 8730
ASSEMBLY NUMBER 10907862-2
REFERENCE DESIGNATOR PREFIX 1A2
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
F1	FUSE 3AGSB 1/8 AMP 250	552001-0001	MDL1/8	71400
J2	CONN, BNC	551100-1094	UG-1094A/U	74868
J2MP1	INSULATOR UG 1094/U BNC	520025-1094	10221N	07047
J2MP2	WASH FIBER FLAT .380.X630X.016	510900-0016	F-7716-380	61000
J101	FILTER LINE 3 AMP 115V-230V	799065-0003	3EF1	05245
TB1	TERM BLK 2TERM 3/8CTR 1.125MT 1/8P	520000-0005	2-176-3	00000
XF1	MIN FUSEHOLDER,R/ANGLE 20AMP S-250V	507002-0003	342004	75915

ASSEMBLY CHASSIS CKT. ASSY 8730
ASSEMBLY NUMBER 20607899-2
REFERENCE DESIGNATOR PREFIX 1A3
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	ASSY MAIN BOARD	10307889-1		24672
A2	PCB ASSY AGC CYCLE DETECTOR	10307878-1		24672
A3	PCB ASSY IRIG A/B READER LOGIC	10307885-1		24672
Q101	30W XSTR SIPNP	7022N4918	2N4918	81349
U101	INT CKT IC	703MC7808U	MC7808CT	04713
W1	CABLE ASSY, RIBBON	11507898		24672
XQ101	CONN TRANSISTOR, 3-PIN FEMALE	551117-0044	10-01-2031	27264
-P1	TERMINAL IC SOCKET 18-24 PIN	551015-9996	08-56-0106	27264
-P2	TERMINAL IC SOCKET 18-24 PIN	551015-9996	08-56-0106	27264
-P3	TERMINAL IC SOCKET 18-24 PIN	551015-9996	08-56-0106	27264
XU101	CONN TRANSISTOR, 3-PIN FEMALE	551117-0044	10-01-2031	27264
-P1	TERMINAL IC SOCKET 18-24 PIN	551015-9996	08-56-0106	27264
-P2	TERMINAL IC SOCKET 18-24 PIN	551015-9996	08-56-0106	27264
-P3	TERMINAL IC SOCKET 18-24 PIN	551015-9996	08-56-0106	27264

5.2. OVERALL FUNCTIONAL DESCRIPTIONS

Refer to the basic block diagram for Model 8730 (Dwg. No. 12307900-02).

5.2.1. Time-of-Year Accumulator (Dwg. No. 12307889-01)

The Time-of-Year (TOY) Accumulator is shown on Sheet 2 of the above schematic. It consists of a presetable, nine-digit counter which accepts the 1 pps update, time bytes and associated strobes from the Reader Logic plus a parallel-in/serial-out shift register. The register develops accumulator serial ONEs for error bypass, display and optional coincidence detection. The counter, which is formed from decades (U23), (U29), (U24), (U30), (U25), (U31), (U26), (U32) and (U27), accumulates time in seconds, minutes, hours and days. Decades (U29) and (U30) are forced to a scale-of-six by gates on (U15) and associated differentiating networks. Decades (U25) and (U31) are forced to a scale-of-twenty-four by an hours reset circuit formed from gate (U15,6) and one-shot (U16,6). The counter is preset to the time contained in the input code under control of the Error Bypass circuit and maintained on-time in forward by the 1 PPS UPDATE through one-shot (U16,10).

Parallel BCD outputs from the counter are fed to the parallel-in/serial-out shift register (U33) through (U38) which outputs serial ONEs in the IRIG format. They are also fed through buffers on (U40) through (U44) to rear panel connector J1 when the parallel BCD output option is included. Buffers on (U39) feed 1 PPS (UPDATE), CARRIER (EC), INHIBIT READ (output from one-shot (U16,10), DC CODE (envelope) and optional coincidence signals to connector J1.

5.2.2. Error Bypass (Dwg. No. 12307889-01)

The Error Bypass circuitry is shown at the upper left on Sheet 1 of the above schematic. The circuit accepts the serial DC Code (envelope) output from the Reader Logic and compares it with the serial ONEs output from the TOY Accumulator. (This is done directly in the case of IRIG time codes. In the case of the XR3 or NASA codes, however, the serial ONEs are first converted to compatible formats on the Reader Logic PCB before being fed to the Error Bypass circuit.) Each bit derived from the accumulator is compared with the corresponding bit from the Reader Logic. If one or more bits within a frame are different, the input frame is assumed to be in error. Mechanically interlocked, front panel, push button switches select zero, two, four or eight frames of Error Bypass and a front panel ERROR indicator lights if an error is detected.

If zero Error Bypass is selected, each input time frame is loaded directly into the accumulator, errors are ignored and the ERROR indicator is not lit. If two, four or eight frames of Error Bypass are selected and the input code is in the forward direction, then two, four or eight consecutive ERROR frames, respectively, are detected before time stripped from the input code loads into the accumulator. The ERROR indicator lights when the selected number of error frames are detected and stays lit until a good frame is verified. When the input code is in the reverse direction, operation is equivalent to zero Error Bypass.

Referring to the schematic, bits are compared in exclusive OR gate (U17,3). The output is strobed by the SAMPLE signal in AND gate (U18,9), which is enabled by the output from flip-flop (U19,1). Flip-flop (U19,1) is set during that portion of the code in which time data are present. If an error is detected, (U18,9) sets flip-flop (U19,13) and the Q output from (U19, 12) clocks counter (U6) when the flip-flop (U19,13) is reset by the 1 ppf signal at the start of the next frame. Counter (U6) counts consecutive error frames. The selected ten-line output is fed through the front panel switch to (U6,13) locking the counter. It is also fed through (U20,4) to the Reader Logic enabling transfer of time data to the accumulator and through (U14,10) to Q1 turning on the front panel ERROR indicator. When a good frame is detected, (U6) is reset by the STOP COMPARE signal through (U18,6) and the process starts over.

5.2.3. Display Control
(Dwg. No. 12307889-01)

The Display Control circuitry is shown on Sheet 1 of the above schematic. The Display Control circuits control the loading of parallel BCD time into the TOY Accumulator shift-register (see 5.2.1) and the clocking of serial ONEs from the register for display, error bypass and optional coincidence detection. The LOAD TIME and Shift Time signals which accomplish this are fed to the shift-register through the Reader Logic PCB (see Section Six). A LOAD TIME pulse is output from (U20,3) at the start of each time code frame, again prior to transfer of serial ONEs to the display and once more after transfer is complete. The SHIFT TIME signal (U5,10) is derived from a free running 80 kHz oscillator (U11,12 and 15) called the Display Clock during transfer of serial ONEs to the display and from the Reader Logic during the remainder of the code frame.

When initiated by a START DISPLAY pulse from the Reader Logic through (U18,10), the Display Control shifts the serial ONEs into shift register (U12) at the DISPLAY CLOCK rate. This is done under control of flip-flop (U21,1) and counter (U13). The output from (U18,10) sets (U21,1) opening gates (U14,3), (U4,10) and closing (U10,4). It resets (U13) enabling it to count DISPLAY CLOCK pulses. At a count of ONE, a LOAD TIME pulse is generated through (U5,4), (U14,3), (U20,3) and the display circuits are reset through C8, R10, (U10,3).

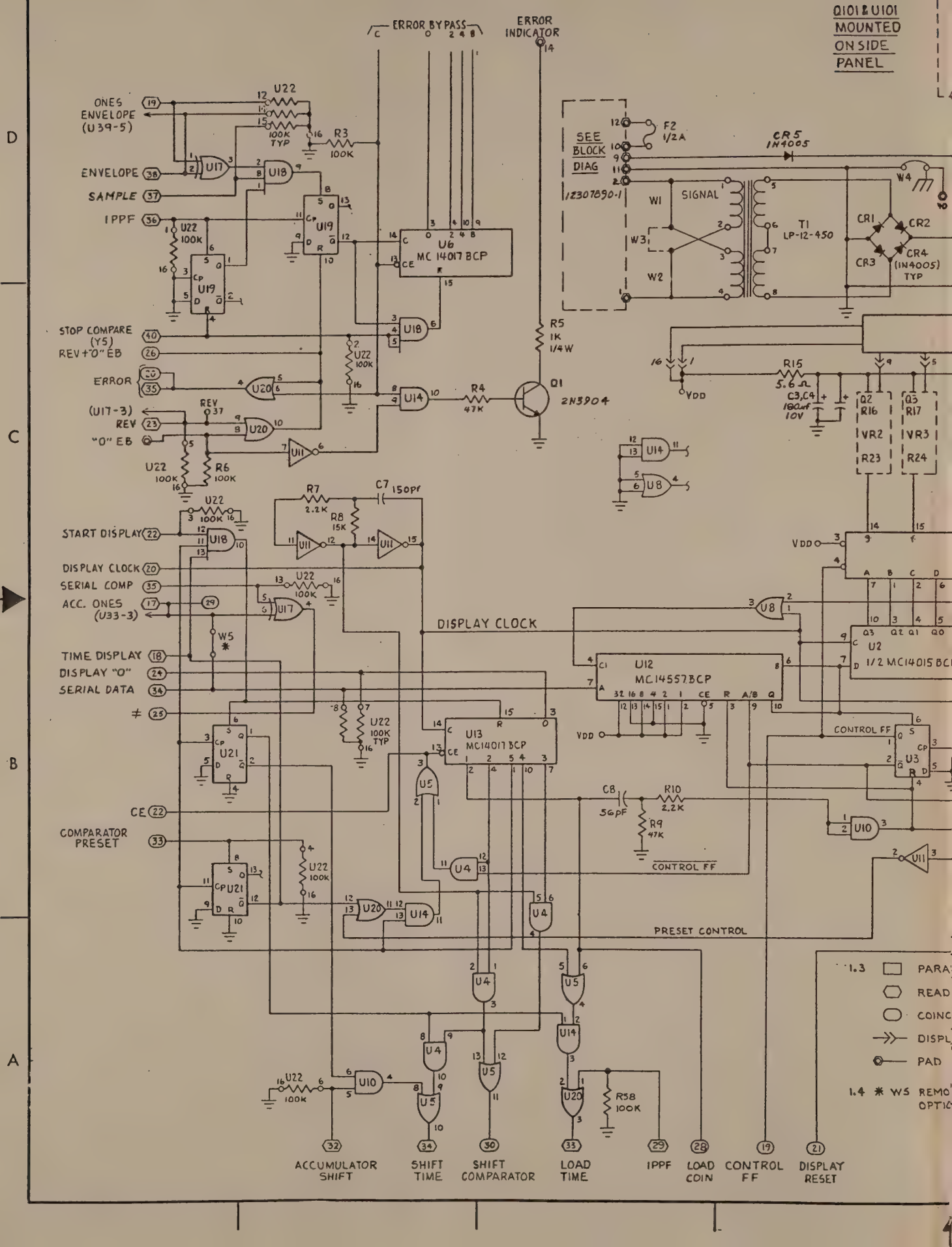
The Q output from control flip-flop (U3,1) enables the A input (U12) and opens gates (U4,3) and (U4,11). The next transition of DISPLAY CLOCK from (U11,12) shifts the first serial ONEs bit (a ONE) into (U12) and the transition following that from (U11,15) steps (U13) to a count of two, removing the enable through (U4,11) and (U5,3). Counter (U13) stays frozen at a count of two until all the serial ONE bits have been loaded into (U12) and the initial ONE output from (U12,10) sets Control flip-flop (U3,1). Counter (U13) is stepped to a count of three, then to four generating a second LOAD TIME pulse through (U5,4), (U14,3) and (U20,3). At step five it opens gates (U14,11), (U18,10) and resets flip-flops (U21,1), (U21,13). The Q output from (U21,13) freezes (U13) through (U20,11), (U14,11), and (U5,3). The circuit is now ready for the next START DISPLAY pulse.

Gate (U10,4) is open and the serial ONEs are clocked by the ACCUMULATOR SHIFT signal from the Reader Logic for use by the Error Bypass circuit. The above activities take place prior to the occurrence of the first time bit in the input code frame. With the Control flip-flop set, the contents of (U12) are recirculated through the B input (the first bit in is the first out) and the reset signals via (U8,11), (U8,10) are removed from counters (U9) and (U7). The bits in (U12) are fed to four-bit serial-in/parallel-out shift register (U2) at the DISPLAY CLOCK rate. Counter (U9) counts bits and transfers them into storage in BCD-to-seven segment drivers (U1) through (U11,4) whenever the state five output from (U9,1) occurs. The bits in (U2) represent a time digit when state five occurs. This same signal resets (U9) through C9, R11, (U8,11) and clocks (U7). Thus counter (U7) counts time digits and the ten-line outputs from (U7) select the display digit. The selected display segments are driven through transistors Q2 through Q8 and the selected digit is enabled by one of the transistors Q9 through Q17. The display is continuously refreshed with the same data until it is again updated by the next START DISPLAY signal.

5.2.4. Power Supply
(Dwg. No. 12307889-01)

The Power Supply is shown at the top of Sheet 1 of the above schematic. The circuit accepts 115 Vac or 230 Vac, 48 Hz to 440 Hz, through rear panel connector, J101, and fuse, F1, and a front panel switch into the primary of T1. It accepts 12 Vdc from rear panel terminal board, TB1, through fuse, F2, and the front panel switch, S2. (Refer to Block Diagram Dwg. No. 12307890-01). Jumpers W1 and W2 must be removed and W3 added to adapt the unit for 230 Vac operation (refer to Section Two). Jumper W4 connects the circuit and chassis ground.

AC, dc or both may be connected to the unit. If both are connected the ac dominates. AC from T1 secondary is rectified by bridge CR1 through CR4 and fed to filter capacitor C1. DC is fed through CR5 to this same point which feeds voltage regulator (U101) and pass transistor Q101. The regulated 8 V from this circuit is fed to the option PCBs and the AGC & Cycle Detector. It also feeds through filter R47, C5 as the Vdd to the Main Board and Display. Zener VR1 and filter R50, C6 establish Vcc (5 V) for the output buffers which feed signals to connector J1. No adjustments are provided.


Q101 & U101 MOUNTED ON SIDE PANEL
ERROR BYPASS
ERROR INDICATOR
ONES ENVELOPE (U39-5)
ENVELOPE
SAMPLE
IPPF
STOP COMPARE (Y5)
REV+"0" EB
ERROR
(U17-3) REV
REV
"0" EB
START DISPLAY
DISPLAY CLOCK
SERIAL COMP
ACC. ONES (U33-3)
TIME DISPLAY
DISPLAY "0"
SERIAL DATA
CE
COMPARATOR PRESET
SEE BLOCK DIAG
1Z307890-1
SIGNAL
T1 LP-12-450
CR1
CR2
CR3
CR4 (1N4005) TYP
CR5 1N4005
F2 1/2A
W1
W2
W3
W4
W5 *
R3 100K
R4 47K
R5 1K 1/4W
R6 100K
R7 2.2K
R8 15K
R9 47K
R10 2.2K
R15 5.6Ω
R16
R17
R23
R24
VR2
VR3
C3,C4 100uf 10V
C7 150pf
C8 56pF
Q1 2N3904
U6 MC 14017 BCP
U12 MC14557BCP
U13 MC14017 BCP
U2 1/2 MC14015 BCP
U3
U5
U8
U10
U11
U14
U17
U18
U19
U20
U21
U22 100K TYP
VDD
CONTROL FF
PRESET CONTROL
ACCUMULATOR SHIFT
SHIFT TIME
SHIFT COMPARATOR
LOAD TIME
IPPF
LOAD COIN
CONTROL FF
DISPLAY RESET

A1	SHOWED DIS OPTION		NFC	12/6/77
B	DISPLAY CONN PIN N°S 10,8,6 WERE 8,6,10	—	11502	12/6/77
C	PER ECO	1001	11503	12/28/77
D	R16-22 WERE 120Ω		11550	1/4/78
E	U4-1,12 & 13 HOOK-UP CHANGED		11616	1/27/78
F	C1 WAS 4000 μf, 35V.		11665	2/14/78
G	C12 & C13 (100μf) WERE 1000μf, ADDED C15 (220μf). (ECR 114-78)		13809	7/21/78
H	R2 WAS 910Ω (ECR 123-78)		13893	8/3/78
J	C7 WAS 330pf ECR 154-80	—	17254	11/20/80
K	CHANGED PER ECO		17918	4/12/81
L	MADE PAD 40 TO C GND; PAD 42 IS NOW C GND.	—	REC	7/12/82
M	R57 WAS 47K, C4 WAS 1000 PF	—	4436	9/21/83
	ADD U4F, DELETED R2, R57, U4I		4615	2/24/84
N	NO. WAS 07188901		4837	

Q101
2N4918

U101
7808
IN OUT
COM

R1
10Ω
1/4W

W6

C1
4700μf
25V

78M05
U45
IN OUT
COM

C2
0.1μf

R49
10Ω
1/4W

C5
1800μf
10V

+5V

VDD

VCC

C6
39μf
10V

38

39

42

DISPLAY

SCHEMATIC # 12307877-1

ASSEMBLY # 10307877-1

Q4 R18 VR4 R25
Q5 R19 VR5 R26
Q6 R20 VR6 R27
Q7 R21 VR7 R28
Q8 2N3904 R22 110Ω R29 5.6K VR8 5.6V IN752
R30 Q9 R39
R31 Q10 R40
R32 Q11 R41
R33 Q12 R42
R34 Q13 R43
R35 Q14 R44
R36 Q15 R45
R37 Q16 R46
R38 16K R47 16K Q17 2N998

U1
MC14511BCP

U11

U10

Y1
X4

U9
MC14017BCP

U7
MC14017BCP

U8

U9

C9
1000pf

R11
2.2k

R12
47k

R13
2.2k

C10
1000 pf

R14
47k

DISPLAY CONTROL

ERROR 17 → 30
COIN IND 5 → 25
CLEAR 27 → 23
COIN(L) 8 → 24
COIN(M) 36 → 33

COINCIDENCE INDICATOR

800 39 → 35
400 40 → 21
200 41 → 29
100 42 → 32

80 50 → 20
40 49 → 27
20 48 → 26
10 47 → 22

COIN PRESET

8 46 → 31
4 45 → 28
2 44 → 15
1 43 → 34

DISPLAY 23 → 36

VDD → 13

U2
1/2 MC14015 BCP

U3

LLEL OUTPUT CONN (J1)

ER CARD CONN (P1,

IDENCE CONN (P2)

AY CARD CONN

VED IF COIN
N INSTALLED

NOTES: (UNLESS OTHERWISE SPECIFIED)

1.1 RESISTORS ARE 1/8W, 5% CARBON COMP.

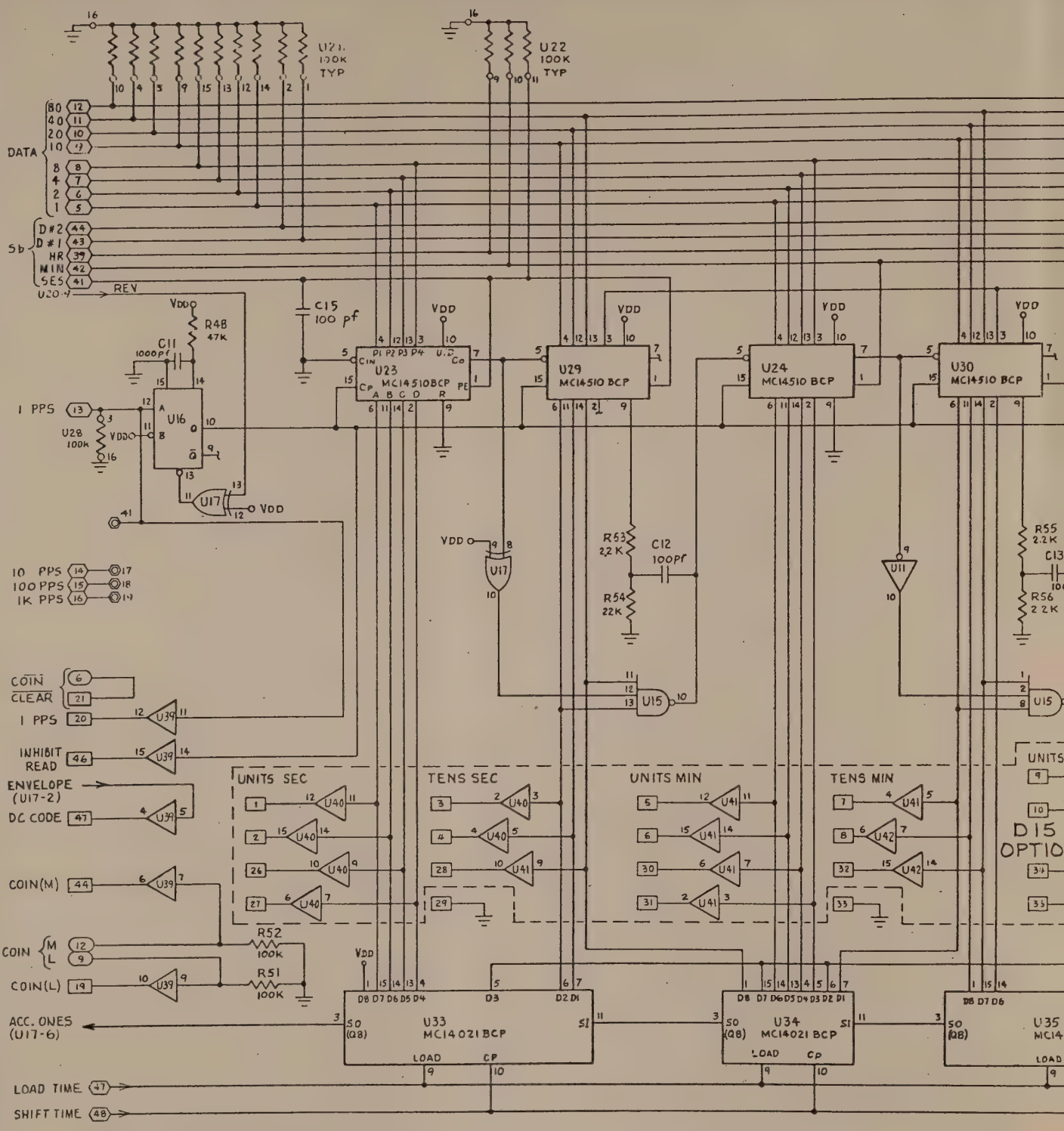
1.2 IC's

IC		TYPE	GND	VDD
U1	MC 14511 BCP	BCD-TO-SEVEN SEGMENT DRIVER	8	16
U2	MC 14015 BCP	DUAL 4-BIT STATIC S.R.	8	16
U3,19,21	MC 14013 BCP	DUAL TYPE D FLIP-FLOP	7	14
U4,10,14	MC 14081 BCP	QUAD 2-INPUT "AND" GATE	7	14
U5,8,20	MC 14071 BCP	QUAD 2-INPUT "OR" GATE	7	14
U6,7,9,13	MC 14017 BCP	DECADE COUNTER/DIVIDER	8	16
U11	MC 14049 BCP	HEX INVERTING BUFFER	8	1
U12	MC 14557 BCP	VARIBLE LENGTH SHIFT REGISTER	8	16
U17	MC 14070 BCP	QUAD EXCLUSIVE "OR" GATE	7	14
U18	MC 14073 BCP	TRIPLE 3-INPUT "AND" GATE	7	14

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

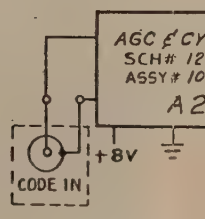
DRAWN J.E.	8-26-77 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	AUSTRON INC AUSTIN, TEXAS
CHECK	DATE	DECIMAL TOLERANCE .X ±.1 .XX ±.01 .XXX ±.005 ANGLES ±	MAIN BOARD - (ERROR BYPASS AND DISPLAY)
ELECT.	DATE		
MECH.	DATE		CODE IDENT. 24672
PROJECT ENG.	DATE		
QA	DATE		
8730	SWMAG+		MATERIAL
USED ON	NEXT ASSY		DRAWING NO. REF 7 SIZE D PART NO. 12307869-1 REV N
APPLICATION		SCALE DO NOT SCALE DRAWING	SH 1 OF 2

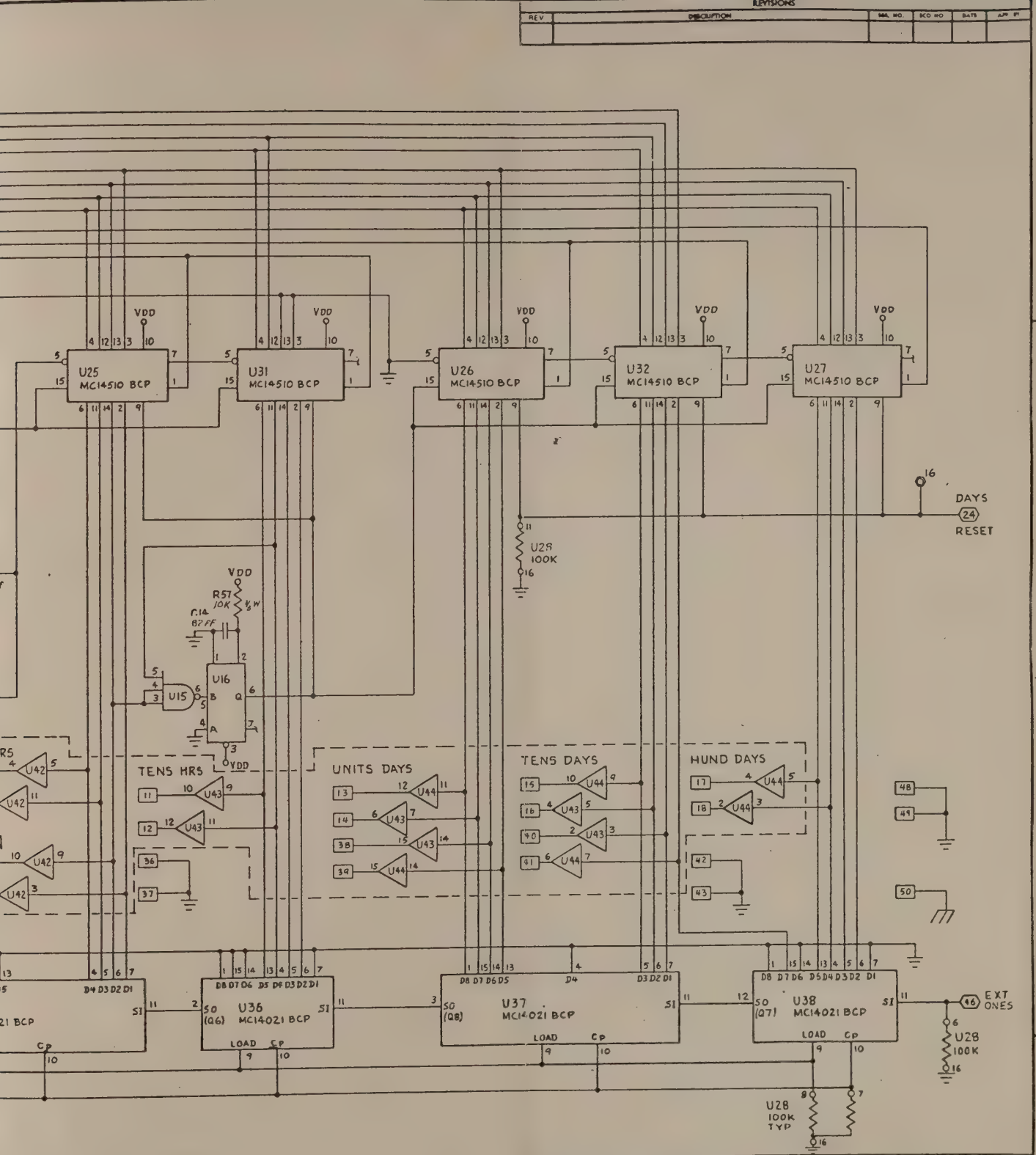


NOTES: (UNLESS OTHERWISE SPECIFIED)

2.1 IC's

IC		TYPE	GND	VDD	VCC
U15	MC 14023 BCP	TRIPLE 3-INPUT "NAND" GATE	7	14	—
U16	MC 14528 BCP	DUAL RETRIGGERABLE ONE-SHOT	8	16	—
U22,28	RES PACK	100K	16	—	—
U23-27,29-32	MC 14510 BCP	BCD UP/DOWN COUNTER	8	16	—
U33-38	MC 14021 BCP	8-BIT STATIC SHIFT REGISTER	8	16	—
U39-44	MC 14050 BCP	HEX NON INVERTING BUFFER	8	—	1





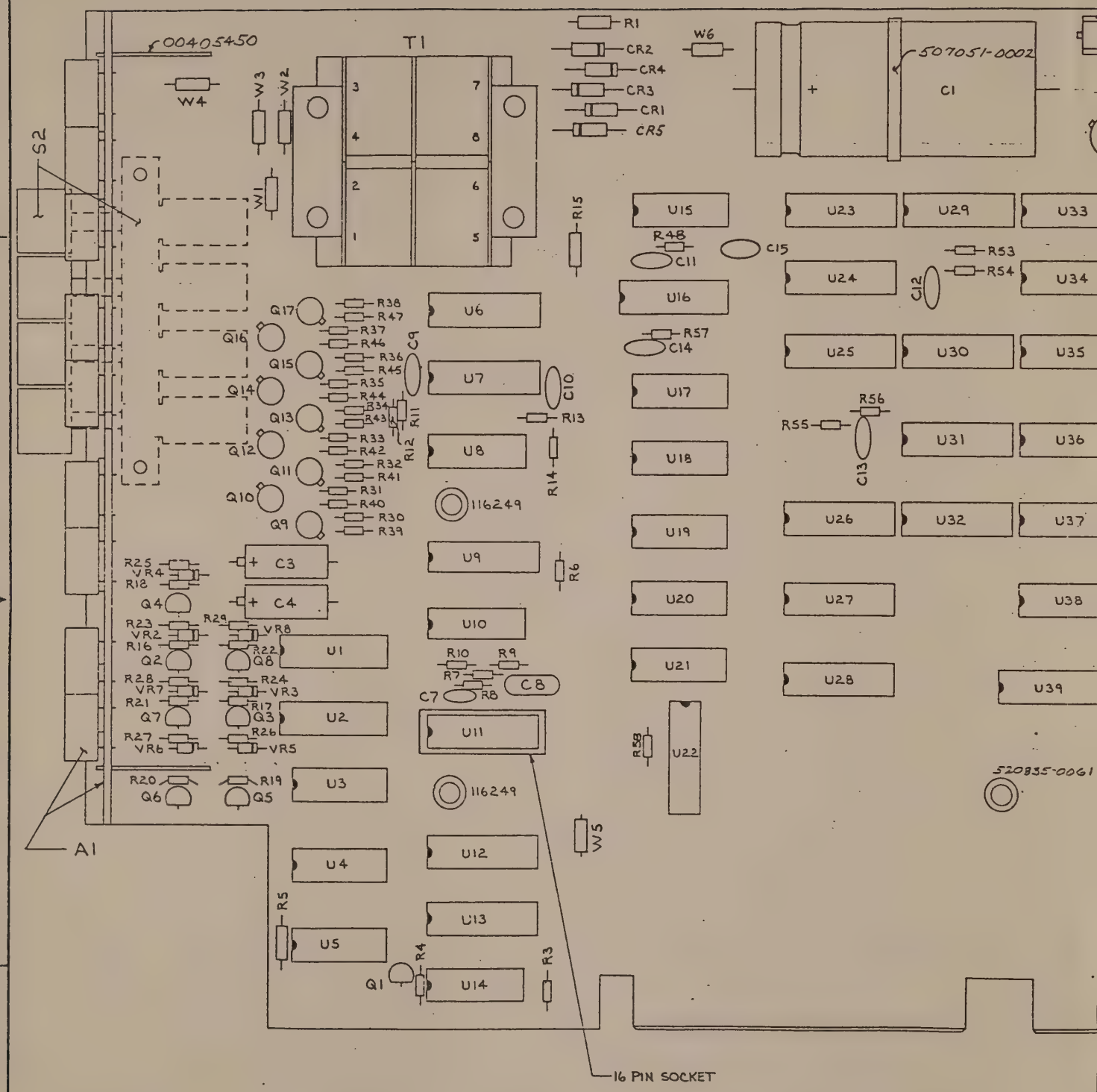
ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN JE	DATE 8-17-77	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	AUSTRON INC. AUSTIN, TEXAS
CHECK	DATE		MAIN BOARD (TIME OF YEAR ACCUMULATOR)
ELECT.	DATE		CODE IDENT. 24672
MECH.	DATE		
PROJECT B. M. 11/77	DATE		
QA	DATE		
8730 USED ON	NEXT ASSY		MATERIA
APPLICATION		SCALE DO NOT SCALE DRAWING	SH 2 OF 2

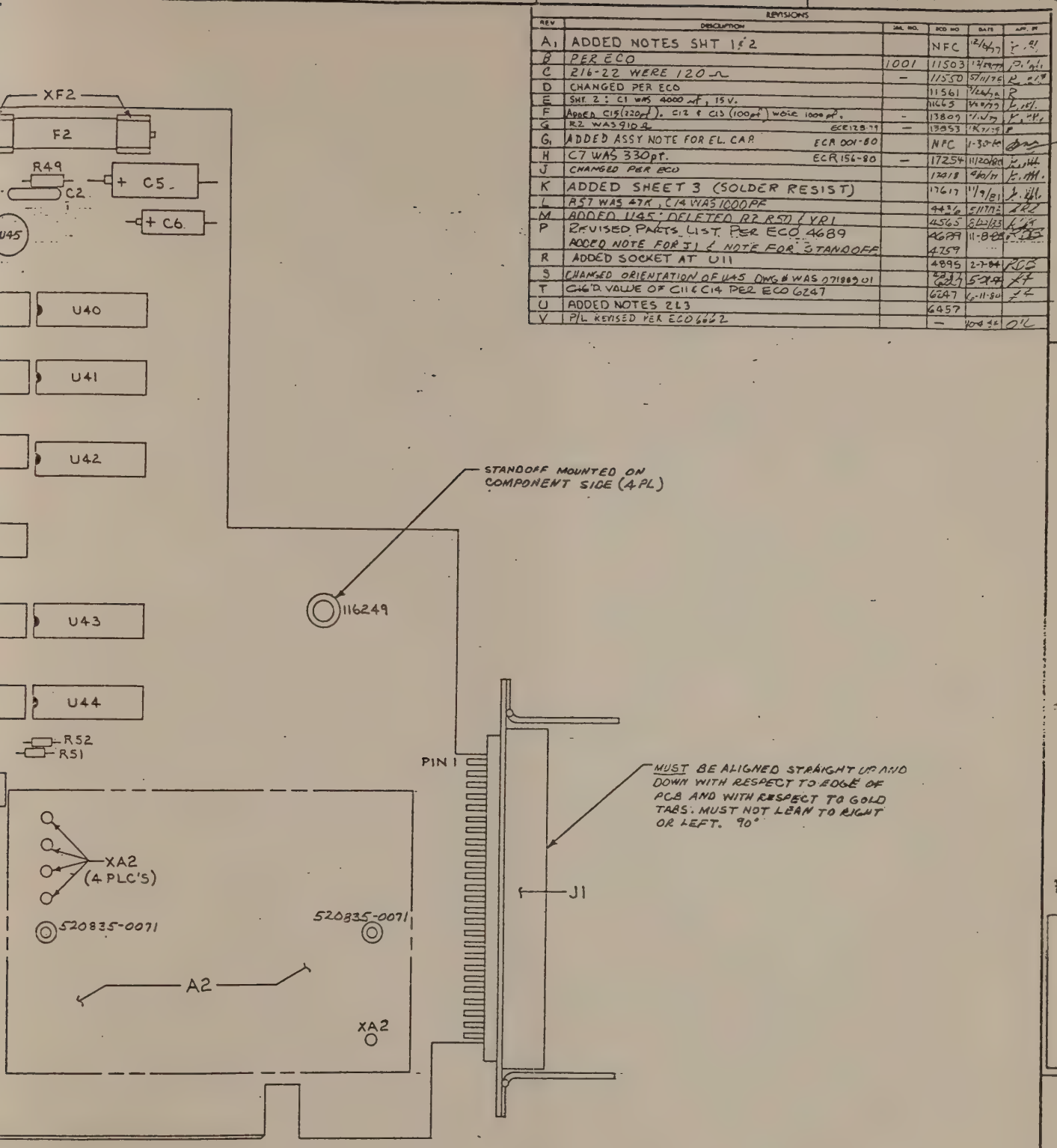
5-14

DRAWING NO. REF	SIZE	PART NO.	REV
7	D	12307889-1	N



3. ADD FOLLOWING JUMPERS TO MAINBOARD ASSY FOR:
   A. BASIC UNIT WITH 110VAC OPERATION: W1,W2,W4,W5,W6.
   B. BASIC UNIT WITH 220VAC OPERATION: W3,W4,W5,W6.
2. IF A17A OPTION IS PRESENT, DELETE W5.
1. U40-U44 INSTALLED WITH D15 OPTION.

NOTES: UNLESS OTHERWISE SPECIFIED



REVISIONS

REV	DESCRIPTION	ENG. NO.	ECO NO	DATE	APP. BY
A1	ADDED NOTES SHT 1 & 2		NFC	12/6/77	
B	PER ECO	1001	11503	1/27/78	
C	216-22 WERE 120 Ω	–	11550	5/11/78	
D	CHANGED PER ECO		11561	7/24/78	
E	SHT. 2: C1 WAS 4000 μf, 15 V.		11663	10/27/78	
F	ADDED C15(220pf). C12 & C13 (100pf) WERE 1000 pf.	–	13809	1/1/79	
G	R2 WAS 910Ω ECR128-79	–	13953	7/1/79	
G1	ADDED ASSY NOTE FOR EL. CAP. ECR 001-80		NFC	1-30-80	
H	C7 WAS 330pf. ECR 156-80	–	17254	11/20/80	
J	CHANGED PER ECO		12018	4/6/81	
K	ADDED SHEET 3 (SOLDER RESIST)		17617	11/9/81	
L	R5T WAS 47K, C14 WAS 1000PF		4496	5/11/82	
M	ADDED U45; DELETED R2 R5 D1 VR1		4565	8/2/83	
P	REVISED PARTS LIST PER ECO 4689 ADDED NOTE FOR J1 & NOTE FOR STANDOFF		4689 4759	11-8-83	
R	ADDED SOCKET AT U11		4895	2-7-84	
S	CHANGED ORIENTATION OF U45 DWG # WAS 071809 01		6227 6247	5-2-84	
T	CHG'D VALUE OF C11 & C14 PER ECO 6247		6247	6-11-84	
U	ADDED NOTES 2 & 3		6457		
V	P/L REVISED PER ECO 6662		–	10-4-84	

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN T.M.H.	DATE 10-11-77	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.1 .XX ±.03 .XXX ±.010 ANGLES ±	AUSTRON INC. AUSTIN, TEXAS	ASSY MAIN BOARD	
CHECK	DATE				
ELECT.	DATE				
MECH.	DATE				
PROJECT	DATE		CODE IDENT. 24672		
QA	DATE				
8730 USED ON	NEXT ASSY	SCALE 2:1	DO NOT SCALE DRAWING	SH 1 OF 3	MATERIAL 5-15
APPLICATION					DRAWING NO. REF D SIZE 10307889-1 DEV V

ASSEMBLY ASSY MAIN BOARD
ASSEMBLY NUMBER 10307889-1
REFERENCE DESIGNATOR PREFIX 1A3A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	PCB ASSY DISPLAY	10307877-1		24672
CR1	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR2	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR3	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR4	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR5	400V 1.5A DIO REC	7011N5395	1N5395	04713
C1	4700UF 25V CAP ELECTROLYTIC	602003-0081	478TTA025A	74840
C2	.1 UF 50V 20 CAP CER DP	601009-0104	2C37Z5U104M050B	56289
C3	180 UF 10V 10CAP TANT	608114-0187	150D187X9010S2	56289
C4	180 UF 10V 10CAP TANT	608114-0187	150D187X9010S2	56289
C5	180 UF 10V 10CAP TANT	608114-0187	150D187X9010S2	56289
C6	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C7	CAP CERA RDL COG 150 PF 200V 5%	605110-0151	C320C151J2G5CA	31433
C8	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C9	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C10	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C11	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C12	100 PF 500V 5 CAP DIP MICA	603000-0101	DM15-101J	02799
C13	100 PF 500V 5 CAP DIP MICA	603000-0101	DM15-101J	02799
C14	82 PF 500V 5 CAP DIP MICA	603000-0820	DM15-820J	02799
C15	100 PF 500V 5 CAP DIP MICA	603000-0101	DM15-101J	02799
F2	FUSE 3AGSB 1/2 AMP 250V	552001-0004	MDL1/2	71400
J1	CONN 50 PIN SOCKET	551306-0051	57-40500	02660
MP1	BRKT DISPLAY & DRIVER BD	00405450		24672
MP2	BRKT DISPLAY & DRIVER BD	00405450		24672
Q1	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q2	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q3	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q4	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q5	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q6	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q7	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q8	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349

ASSEMBLY ASSY MAIN BOARD (CONT)
ASSEMBLY NUMBER 10307889-1
REFERENCE DESIGNATOR PREFIX 1A3A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
Q9	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q10	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q11	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q12	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q13	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q14	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q15	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q16	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
Q17	500MW 60V XSTR NPN DARLINGTON TO-72	7022N998	2N998	04713
R1	RES FXD COMP 10 OHM 1/4W 10%	651102-0100	RC07GF100K	81349
R3	RES FXD COMP 100 K 1/8W 10%	651110-0104	RC05GF104K	81349
R4	RES FXD COMP 47 K 1/8W 05%	651111-0473	RC05GF473J	81349
R5	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R6	RES FXD COMP 100 K 1/8W 10%	651110-0104	RC05GF104K	81349
R7	RES FXD COMP 2.2 K 1/8W 10%	651110-0222	RC05GF222K	81349
R8	RES FXD COMP 15 K 1/8W 10%	651110-0153	RC05GF153K	81349
R9	RES FXD COMP 47 K 1/8W 05%	651111-0473	RC05GF473J	81349
R10	RES FXD COMP 2.2 K 1/8W 10%	651110-0222	RC05GF222K	81349
R11	RES FXD COMP 2.2 K 1/8W 10%	651110-0222	RC05GF222K	81349
R12	RES FXD COMP 47 K 1/8W 05%	651111-0473	RC05GF473J	81349
R13	RES FXD COMP 2.2 K 1/8W 10%	651110-0222	RC05GF222K	81349
R14	RES FXD COMP 47 K 1/8W 05%	651111-0473	RC05GF473J	81349
R15	RES FXD COMP 5.6 OHM 1/4W 10%	651102-05R6	RC07GF5R6K	81349
R16	RES FXD COMP 110 OHM 1/8W 05%	651111-0111	RC05GF111J	81349
R17	RES FXD COMP 110 OHM 1/8W 05%	651111-0111	RC05GF111J	81349
R18	RES FXD COMP 110 OHM 1/8W 05%	651111-0111	RC05GF111J	81349
R19	RES FXD COMP 110 OHM 1/8W 05%	651111-0111	RC05GF111J	81349
R20	RES FXD COMP 110 OHM 1/8W 05%	651111-0111	RC05GF111J	81349
R21	RES FXD COMP 110 OHM 1/8W 05%	651111-0111	RC05GF111J	81349
R22	RES FXD COMP 110 OHM 1/8W 05%	651111-0111	RC05GF111J	81349
R23	RES FXD COMP 5.6 K 1/8W 10%	651110-0562	RC05GF562K	81349
R24	RES FXD COMP 5.6 K 1/8W 10%	651110-0562	RC05GF562K	81349
R25	RES FXD COMP 5.6 K 1/8W 10%	651110-0562	RC05GF562K	81349

ASSEMBLY ASSY MAIN BOARD (CONT)
ASSEMBLY NUMBER 1030789-1
REFERENCE DESIGNATOR PREFIX 1A3A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R26	RES FXD COMP 5.6 K 1/8W 10%	651110-0562	RC05GF562K	81349
R27	RES FXD COMP 5.6 K 1/8W 10%	651110-0562	RC05GF562K	81349
R28	RES FXD COMP 5.6 K 1/8W 10%	651110-0562	RC05GF562K	81349
R29	RES FXD COMP 5.6 K 1/8W 10%	651110-0562	RC05GF562K	81349
R30	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R31	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R32	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R33	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R34	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R35	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R36	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R37	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R38	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R39	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R40	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R41	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R42	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R43	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R44	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R45	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R46	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R47	RES FXD COMP 16 K 1/8W 05%	651111-0163	RC05GF163J	81349
R48	RES FXD COMP 47 K 1/8W 05%	651111-0473	RC05GF473J	81349
R49	RES FXD COMP 10 OHM 1/4W 10%	651102-0100	RC07GF100K	81349
R51	RES FXD COMP 100 K 1/8W 10%	651110-0104	RC05GF104K	81349
R52	RES FXD COMP 100 K 1/8W 10%	651110-0104	RC05GF104K	81349
R53	RES FXD COMP 2.2 K 1/8W 10%	651110-0222	RC05GF222K	81349
R54	RES FXD COMP 22 K 1/8W 10%	651110-0223	RC05GF223K	81349
R55	RES FXD COMP 2.2 K 1/8W 10%	651110-0222	RC05GF222K	81349
R56	RES FXD COMP 22 K 1/8W 10%	651110-0223	RC05GF223K	81349
R57	RES FXD COMP 10 K 1/8W 10%	651110-0103	RC05GF103K	81349
R58	RES FXD COMP 100 K 1/8W 10%	651110-0104	RC05GF104K	81349
S2	SWITCH, PUSHBUTTON, 2PDT 4POS	553909-1250	F12.5042UGRB140101BA	00000

ASSEMBLY ASSY MAIN BOARD (CONT)
ASSEMBLY NUMBER 10307889-1
REFERENCE DESIGNATOR PREFIX 1A3A1
QUANTITY 1 EA

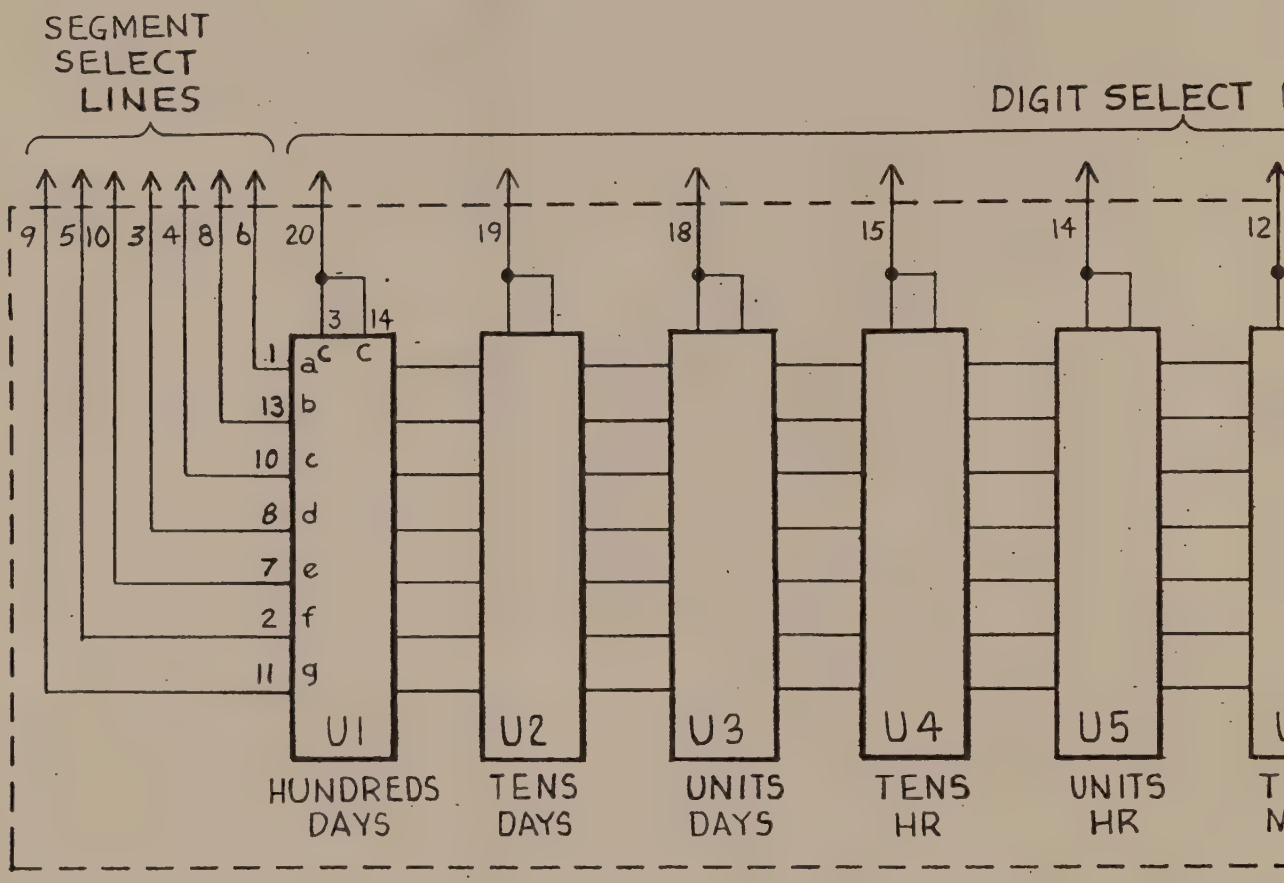
REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
T1	XFMR POWER 115V PRI 12.6V CT 450MA	751310-0450	LP-12-450	08779
U1	IC CMOS BCD-7SEG LATCH/DECODE/DR	703MC145118P	MC145118CP	04713
U2	IC CMOS 2*4BIT STATIC SR 16	703MC140156P	MC140156CP	04713
U3	IC CMOS DUAL D F/F,IN D,CLK	703MC140136P	MC140136CP	04713
U4	IC CMOS 4-2IN AND 14DIP	703MC140816P	MC140816CP	04713
U5	IC CMOS 4 2IN OR 14DIP	703MC140716P	MC140716CP	04713
U6	IC CMOS DEC CNTR 5STAGE JOH	703MC140176P	MC140176CP	04713
U7	IC CMOS DEC CNTR 5STAGE JOH	703MC140176P	MC140176CP	04713
U8	IC CMOS 4 2IN OR 14DIP	703MC140716P	MC140716CP	04713
U9	IC CMOS DEC CNTR 5STAGE JOH	703MC140176P	MC140176CP	04713
U10	IC CMOS 4-2IN AND 14DIP	703MC140816P	MC140816CP	04713
U11	IC CMOS HEX INV/BUFF	703MC140496P	MC140496UBCP	04713
U12	IC CMOS VAR LENGTH SHIFT REG	703MC145576C	MC145576CP	04713
U13	IC CMOS DEC CNTR 5STAGE JOH	703MC140176P	MC140176CP	04713
U14	IC CMOS 4-2IN AND 14DIP	703MC140816P	MC140816CP	04713
U15	IC CMOS 3*3IN NAND	703MC140236P	MC140236CP	04713
U16	IC CMOS DUAL MONOSTBL MULTI	703MC145286P	MC145286CP	04713
U17	IC CMOS EXCLUSIVE OR GATES	703MC140706P	MC140706CP	04713
U18	IC CMOS 3*3IN AND	703CD4073BE	CD4073BE	02735
U19	IC CMOS DUAL D F/F,IN D,CLK	703MC140136P	MC140136CP	04713
U20	IC CMOS 4 2IN OR 14DIP	703MC140716P	MC140716CP	04713
U21	IC CMOS DUAL D F/F,IN D,CLK	703MC140136P	MC140136CP	04713
U22	RES FXD DIPNET 16 100 K 1.75W 2%	654010-0104	316A104	01121
U23	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U24	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U25	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U26	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U27	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U28	RES FXD DIPNET 16 100 K 1.75W 2%	654010-0104	316A104	01121
U29	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U30	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U31	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713
U32	IC CMOS BCD-PRST UP-DWN CNTR	703MC145108P	MC145108CP	04713

ASSEMBLY ASSY MAIN BOARD (CONT)
ASSEMBLY NUMBER 10307889-1
REFERENCE DESIGNATOR PREFIX 1A3A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U33	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U34	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U35	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U36	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U37	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U38	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U39	IC CMOS HEX BUFFER	703MC14050BP	MC14050BCP	04713
U40	SEE OPTION (D15)			
U41	SEE OPTION (D15)			
U42	SEE OPTION (D15)			
U43	SEE OPTION (D15)			
U44	SEE OPTION (D15)			
VR2	5.6 V 400MW 5.0 DIO S ZEN DO-7	7011N752A	1N752A	08288
VR3	5.6 V 400MW 5.0 DIO S ZEN DO-7	7011N752A	1N752A	08288
VR4	5.6 V 400MW 5.0 DIO S ZEN DO-7	7011N752A	1N752A	08288
VR5	5.6 V 400MW 5.0 DIO S ZEN DO-7	7011N752A	1N752A	08288
VR6	5.6 V 400MW 5.0 DIO S ZEN DO-7	7011N752A	1N752A	08288
VR7	5.6 V 400MW 5.0 DIO S ZEN DO-7	7011N752A	1N752A	08288
VR8	5.6 V 400MW 5.0 DIO S ZEN DO-7	7011N752A	1N752A	08288
W1	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W2	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W4	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W5	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W6	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
XA2-1	SOCKET, PIN	551331-0403	PS403-30	00000
XA2-2	SOCKET, PIN	551331-0403	PS403-30	00000
XA2-3	SOCKET, PIN	551331-0403	PS403-30	00000
XA2-4	SOCKET, PIN	551331-0403	PS403-30	00000
XA2-5	SOCKET, PIN	551331-0403	PS403-30	00000
XF2-A	CLIP FUSE SINGLE PC/MT	552007-0000	102071	75915
XF2-B	CLIP FUSE SINGLE PC/MT	552007-0000	102071	75915

5.2.5. Display
(Dwg. No. 12307877-01)

The display consists of nine, seven-segment, LED digits with the segments wired in parallel. Separate digit select lines are provided. LED colons are provided between days and hours, hours and minutes and minutes and seconds.



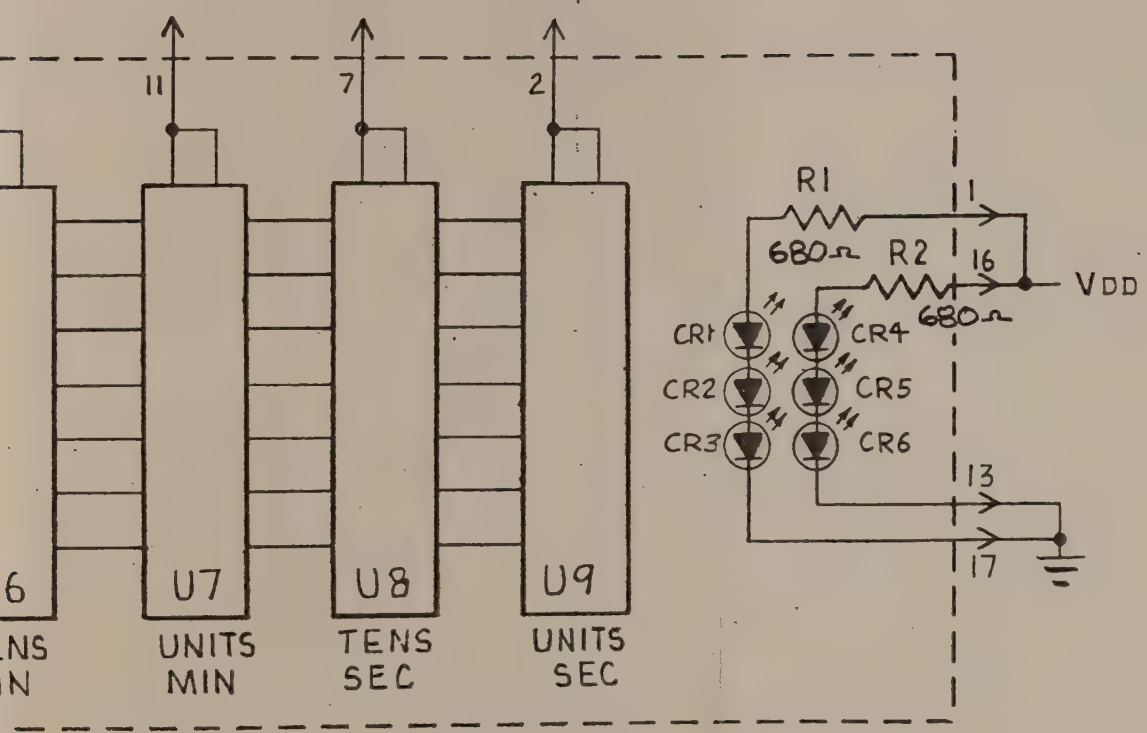
NOTES:(UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE 1/8W, 5%, CARBON COMP.
2. DIODES ARE HP 5082-4480.
3. U1-U9 ARE HP 5082-7653.

REVISIONS					
REV	DESCRIPTION	ECR NO.	ECO NO.	DATE	APP. BY
A					
B	CONN Nº5 10,8,6 / UI Nº3 1/13 WERE 8,6,10,13,1	—	11502	4/4/77	
C	R1,2 WERE 1K		11550	5/78	
D	CHANGED: CR1-6 TYPE; R1, R2 VALUE -	-	11623	11/1/81	
E	DWG NO. WAS 07187701		4837		

D

INES



C

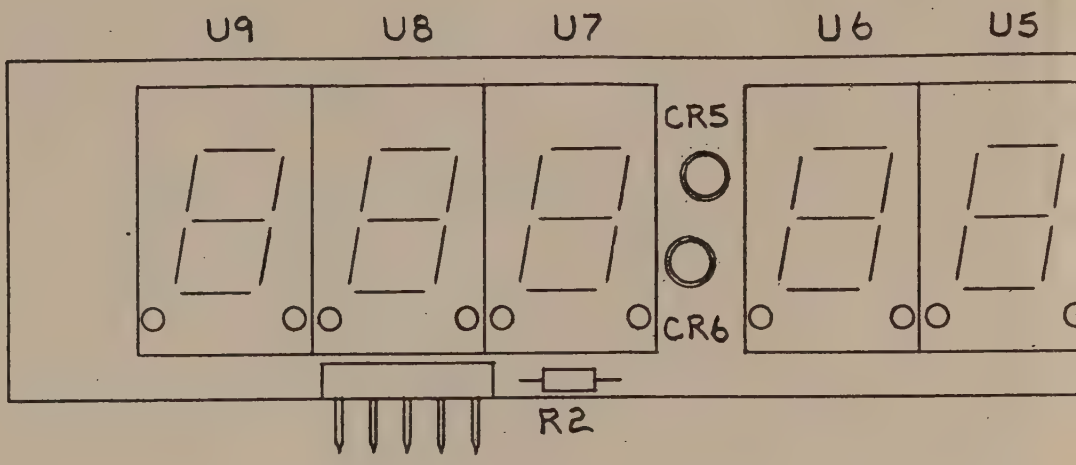
B

A

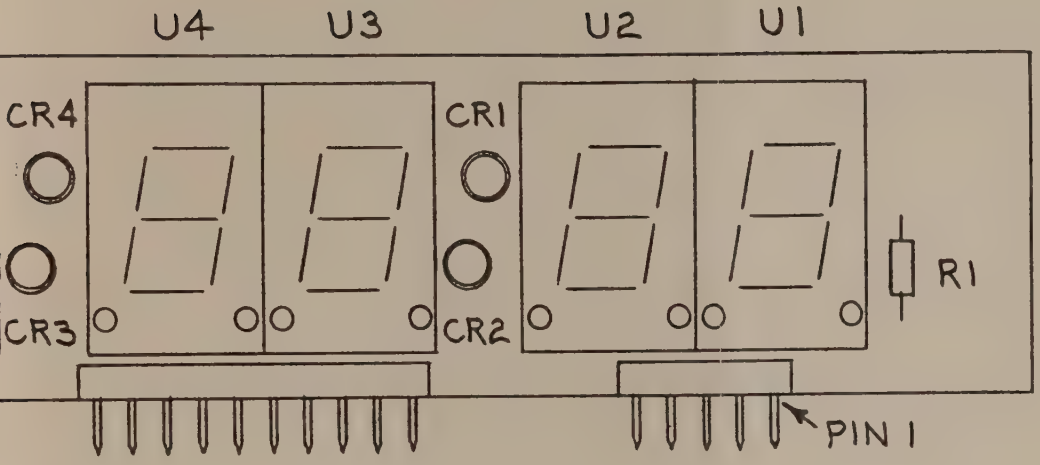
ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN J.C. 10-17-77 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	AUSTRON AUSTIN, TEXAS	DISPLAY SCHEMATIC
CHECK DATE			
ELECT. DATE			
MECH. DATE		CODE IDENT 24672	
QA DATE			
8730 USED ON / NEXT ASSY	SCALE / DO NOT SCALE DRAWING	MATERIAL	DRAWING NO. REF / SIZE / PART NO. / REV.
APPLICATION	SH 1 OF 1	5-22	B 12307877-1 E


U9
U8
U7
U6
U5
CR5
CR6
R2

REVISIONS					
REV	DESCRIPTION	PER. NO.	ECO NO.	DATE	APP. BY
A1	CHG'D RES ON SHT 2		NFC	11/22/77	
A2	CORRECTED ORIENTATION CR1-6	-	NFC	11/28/78	R
B	R1,2 WERE 1K	-	11550	5/7/81	R&M
C	DIODES WERE 100455. R1,2 WERE 1.2K	-	17623	12/3/81	H.W.
D	DWG NO. WAS 07187701		4837		
E	REV PER ECO 6937		6937	11/05	



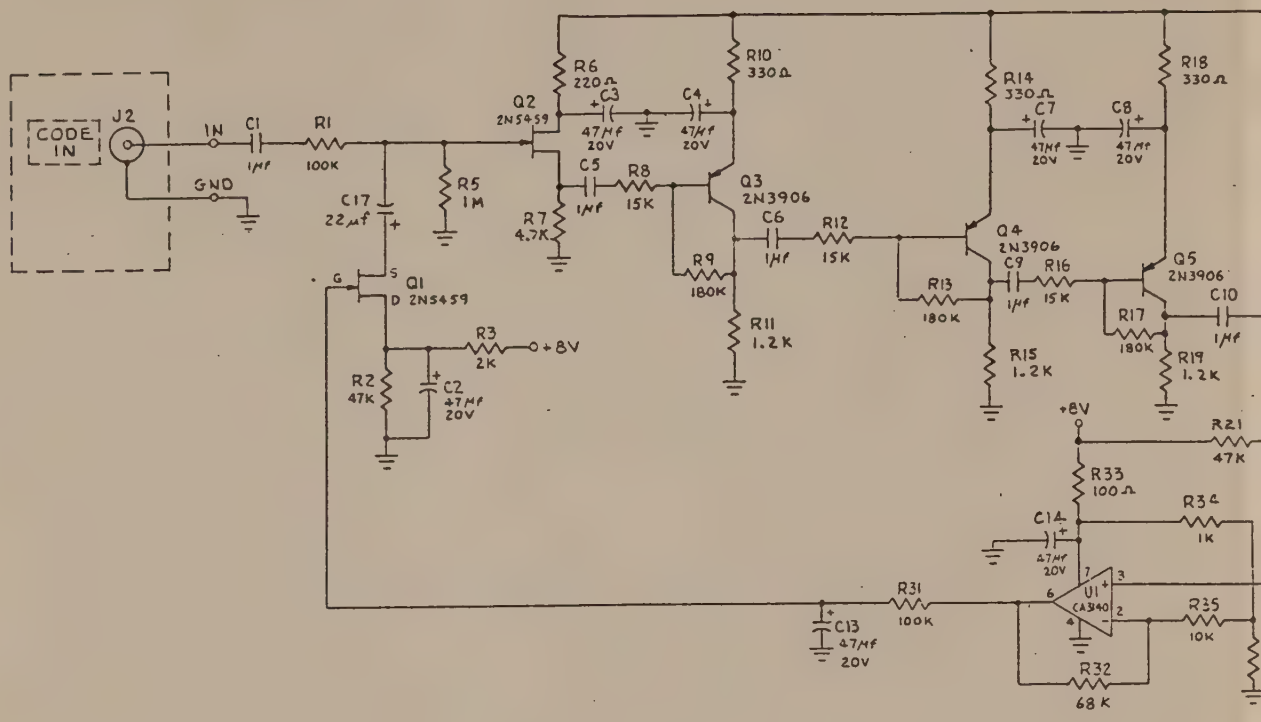
ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN T.M.H. 10-5-77	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	AUSTRON AUSTIN, TEXAS	ASSY DISPLAY BOARD
CHECK DATE			
ELECT. DATE			
MECH. DATE		CODE IDENT 24672	
PROJECT MGR. 12/19 DATE			
QA DATE		MATERIAL 5-23	DRAWING NO. REF B 10307877-1 REV E
8730 USED ON / NEXT ASSY			
APPLICATION	SCALE 2:1 / DO NOT SCALE DRAWING / SH 1 OF 2		

ASSEMBLY PCB ASSY DISPLAY
ASSEMBLY NUMBER 10307877-1
REFERENCE DESIGNATOR PREFIX 1A3A1A1
QUANTITY 1 EA

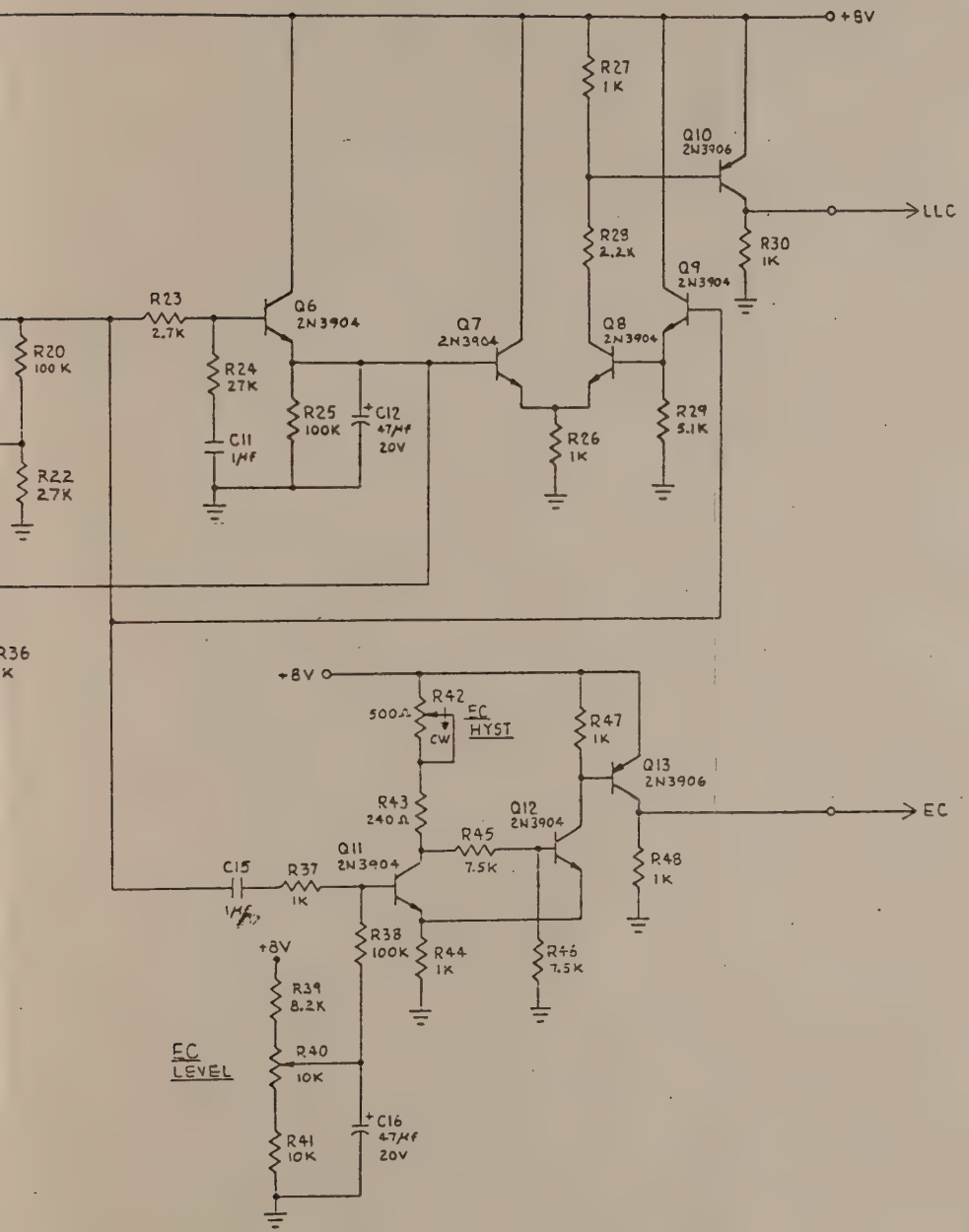
REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR1MP1	1/8LX3/16 SPACER ROUND NYLON	520821-0005	9207N-115	06540
CR2	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR2MP1	1/8LX3/16 SPACER ROUND NYLON	520821-0005	9207N-115	06540
CR3	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR3MP1	1/8LX3/16 SPACER ROUND NYLON	520821-0005	9207N-115	06540
CR4	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR4MP1	1/8LX3/16 SPACER ROUND NYLON	520821-0005	9207N-115	06540
CR5	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR5MP1	1/8LX3/16 SPACER ROUND NYLON	520821-0005	9207N-115	06540
CR6	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR6MP1	1/8LX3/16 SPACER ROUND NYLON	520821-0005	9207N-115	06540
R1	RES FXD COMP 680 OHM 1/8W 10%	651110-0681	RC05GF681K	81349
R2	RES FXD COMP 680 OHM 1/8W 10%	651110-0681	RC05GF681K	81349
U1	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U2	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U3	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U4	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U5	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U6	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U7	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U8	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
U9	LED RED 7SEG COMMON CATH	555600-7653	5082-7653	28480
XA1	CONN 30 PIN RT ANGLE MALE	551009-0045	200264	16512



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE 1/8 W, 5%, CARBON COMP.

REVISIONS					
REV	DESCRIPTION	ENG. NO.	ECO NO.	DATE	APP'D
A1	C3 & C14 WERE C1 & C4		NEC	4/23/79	[illegible]
B	CHG'D VALUES OF R7, 27, 28, 39 & Q7 & +9/+12V TO +8V	1001	11506	4/14/77	[illegible]
C	DELETED R6 (1000Ω). ADDED C17 (33pf). (CHANGED R5, R6, R19, R23, R27, R32 VALUES. (CHG 075-00 TO 100Ω)	-	13904	4/6/80	[illegible]
D	DWG NO. WAS 07187801		4837	8/01/84	[illegible]



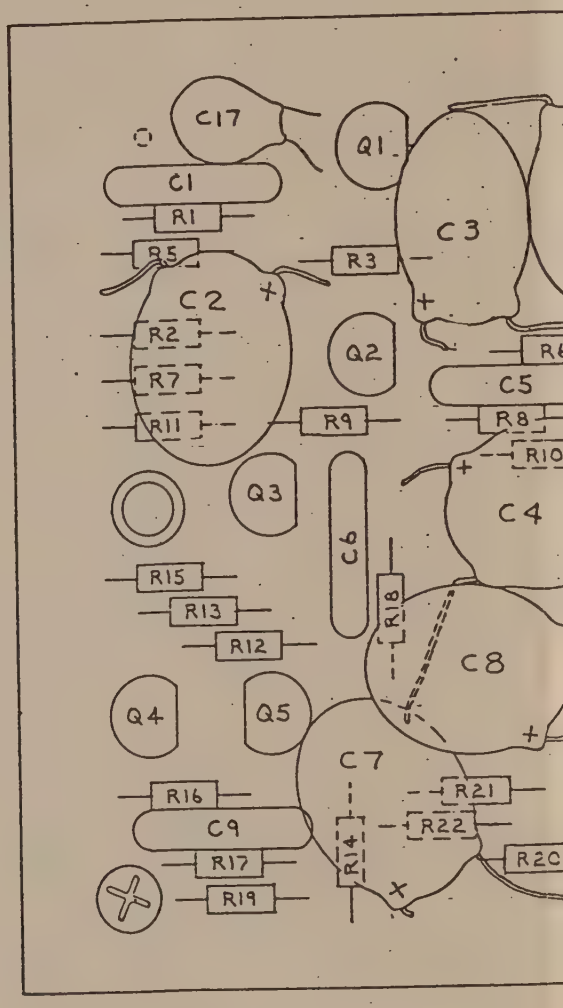
ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN JCE 10-13-77 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	AUSTRON INC. AUSTIN, TEXAS	AGC & CYCLE DETECTOR
CHECK DATE			
ELECT. DATE			
MECH. DATE			
PROJECT [illegible] DATE		CODE IDENT. 24672	
QA DATE			
8730 USED ON / NEXT ASSY	DO NOT SCALE DRAWING	MATERIAL	DRAWING NO. REF D SIZE 12307878-1 REV D
APPLICATION	SCALE SH 1 OF 1		

4 3

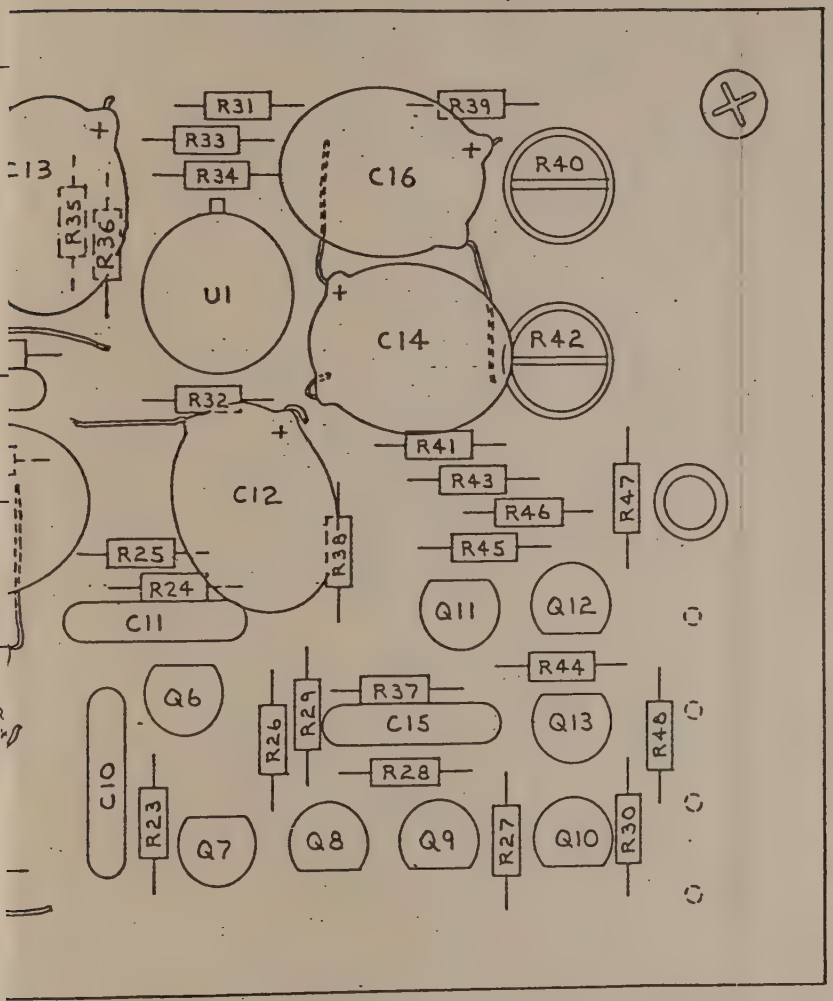
D C B A



NOTES:

1. COMPONENT HEIGHT NOT TO EXCEED SPACER HEIGHT
2. SHIELD 081241 IS MOUNTED ON FAR SIDE.

REVISIONS					
REV	DESCRIPTION	ENG. NO.	ECO NO.	DATE	APP. BY
A	Released To Records			12/16/71	
B	CHG'D VALUES OF R7, 27, 28, & 39 ON SHT 3 of 6	1001	11506	4/11/77	G. M.
C	DELETED R4; ADDED C17; CHANGED VALUES R5, R11, R15, R19, R21, R27.		13904	9/1/80	G. M.
D	CHANGED C2, C3, C4, C7, C8, C12, C13, C14, C16, SPACERS, COVER.		17099	7/30/80	G. M.
E	DWG NO. WAS 07187801		4837		
F	P/L CHG ONLY		6399	5/5/82	RKS



ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN T.M.H. 12-1-77	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	AUSTRON INC. AUSTIN, TEXAS	ASSY AGC & CYCLE DETECTOR	
CHECK	DATE				
ELECT.	DATE				
MECH.	DATE				
PROJECT R.M. 12/7	DATE		CODE IDENT. 24672		
QA	DATE				
8730			MATERIAL	DRAWING NO.	REV
USED ON	NEXT ASSY			REF SIZE PART NO.	
APPLICATION			5-27	C 10307878-1	F
SCALE 4:1	DO NOT SCALE DRAWING	SH 1 OF 7			

ASSEMBLY PCB ASSY AGC CYCLE DETECTOR
ASSEMBLY NUMBER 10307878-1
REFERENCE DESIGNATOR PREFIX 1A3A2
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	1 UF 50V CAP CER DP	601009-0105	2C37Z5U105M050B	56289
C2	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C3	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C4	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C5	1 UF 50V CAP CER DP	601009-0105	2C37Z5U105M050B	56289
C6	1 UF 50V CAP CER DP	601009-0105	2C37Z5U105M050B	56289
C7	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C8	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C9	1 UF 50V CAP CER DP	601009-0105	2C37Z5U105M050B	56289
C10	1 UF 50V CAP CER DP	601009-0105	2C37Z5U105M050B	56289
C11	1 UF 50V CAP CER DP	601009-0105	2C37Z5U105M050B	56289
C12	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C13	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C14	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C15	1 UF 50V CAP CER DP	601009-0105	2C37Z5U105M050B	56289
C16	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C17	22 UF 10V 10 CAP TANT	608114-0226	196D226X9010JA1	56289
J2-1	CONN PIN, SWAGE .040DX.50L	520022-0000	460-2946-02-03	
J2-2	CONN PIN, SWAGE .040DX.50L	520022-0000	460-2946-02-03	
J2-3	CONN PIN, SWAGE .040DX.50L	520022-0000	460-2946-02-03	
J2-4	CONN PIN, SWAGE .040DX.50L	520022-0000	460-2946-02-03	
J2-5	CONN PIN, SWAGE .040DX.50L	520022-0000	460-2946-02-03	
MP1	COVER MOD	00707879-3		24672
MP2	SHIELD	01208241		24672
MP3	SCREW 2-56X5/16 FLAT HD PHIL B-OXID	400011-0000		
MP4	SCREW 2-56X5/16 FLAT HD PHIL B-OXID	400011-0000		
Q1	TO-92 XSTR JFET	7022N5459	2N5459	04713
Q2	TO-92 XSTR JFET	7022N5459	2N5459	04713
Q3	0.31W TO-92 XSTR PNPS SM	7022N3906	2N3906	81349
Q4	0.31W TO-92 XSTR PNPS SM	7022N3906	2N3906	81349
Q5	0.31W TO-92 XSTR PNPS SM	7022N3906	2N3906	81349
Q6	0.31W TO-92 XSTR NPNS SM	7022N3904	2N3904	81349
Q7	0.31W TO-92 XSTR NPNS SM	7022N3904	2N3904	81349

ASSEMBLY PCB ASSY AGC CYCLE DETECTOR (CONT)
ASSEMBLY NUMBER 10307878-1
REFERENCE DESIGNATOR PREFIX 1A3A2
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
Q8	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q9	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q10	0.31W TO-92 XSTR PNPS SH	7022N3906	2N3906	81349
Q11	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q12	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q13	0.31W TO-92 XSTR PNPS SH	7022N3906	2N3906	81349
R1	RES FXD COMP 100 K 1/8W 05%	651111-0104	RC05GF104J	81349
R2	RES FXD COMP 47 K 1/8W 05%	651111-0473	RC05GF473J	81349
R3	RES FXD COMP 2 K 1/8W 05%	651111-0202	RC05GF202J	81349
R5	RES FXD COMP 1 M 1/8W 05%	651111-0105	RC05GF105J	81349
R6	RES FXD COMP 220 OHM 1/8W 05%	651111-0221	RC05GF221J	81349
R7	RES FXD COMP 4.7 K 1/8W 05%	651111-0472	RC05GF472J	81349
R8	RES FXD COMP 15 K 1/8W 05%	651111-0153	RC05GF153J	81349
R9	RES FXD COMP 180 K 1/8W 05%	651111-0184	RC05GF184J	81349
R10	RES FXD COMP 330 OHM 1/8W 05%	651111-0331	RC05GF331J	81349
R11	RES FXD COMP 1.2 K 1/8W 05%	651111-0122	RC05GF122J	81349
R12	RES FXD COMP 15 K 1/8W 05%	651111-0153	RC05GF153J	81349
R13	RES FXD COMP 180 K 1/8W 05%	651111-0184	RC05GF184J	81349
R14	RES FXD COMP 330 OHM 1/8W 05%	651111-0331	RC05GF331J	81349
R15	RES FXD COMP 1.2 K 1/8W 05%	651111-0122	RC05GF122J	81349
R16	RES FXD COMP 15 K 1/8W 05%	651111-0153	RC05GF153J	81349
R17	RES FXD COMP 180 K 1/8W 05%	651111-0184	RC05GF184J	81349
R18	RES FXD COMP 330 OHM 1/8W 05%	651111-0331	RC05GF331J	81349
R19	RES FXD COMP 1.2 K 1/8W 05%	651111-0122	RC05GF122J	81349
R20	RES FXD COMP 100 K 1/8W 05%	651111-0104	RC05GF104J	81349
R21	RES FXD COMP 47 K 1/8W 05%	651111-0473	RC05GF473J	81349
R22	RES FXD COMP 27 K 1/8W 05%	651111-0273	RC05GF273J	81349
R23	RES FXD COMP 2.7 K 1/8W 05%	651111-0272	RC05GF272J	81349
R24	RES FXD COMP 27 K 1/8W 05%	651111-0273	RC05GF273J	81349
R25	RES FXD COMP 100 K 1/8W 05%	651111-0104	RC05GF104J	81349
R26	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R27	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R28	RES FXD COMP 2.2 K 1/8W 05%	651111-0222	RC05GF222J	81349

ASSEMBLY PCB ASSY AGC CYCLE DETECTOR (CONT)
ASSEMBLY NUMBER 10307878-1
REFERENCE DESIGNATOR PREFIX 1A3A2
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R29	RES FXD COMP 5.1 K 1/8W 05%	651111-0512	RC05GF512J	81349
R30	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R31	RES FXD COMP 100 K 1/8W 05%	651111-0104	RC05GF104J	81349
R32	RES FXD COMP 68 K 1/8W 05%	651111-0683	RC05GF683J	81349
R33	RES FXD COMP 100 OHM 1/8W 05%	651111-0101	RC05GF101J	81349
R34	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R35	RES FXD COMP 10 K 1/8W 05%	651111-0103	RC05GF103J	81349
R36	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R37	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R38	RES FXD COMP 100 K 1/8W 05%	651111-0104	RC05GF104J	81349
R39	RES FXD COMP 8.2 K 1/8W 05	651111-0822	RC05GF822J	81349
R40	10 K 1/2W 20 POT 1T PC CERM	659009-1103	3329H-1-103	80294
R41	RES FXD COMP 10 K 1/8W 05%	651111-0103	RC05GF103J	81349
R42	500 OHM 1/2W 20 POT 1T PC CERM	659009-1501	3329H-1-501	80294
R43	RES FXD COMP 240 OHM 1/8W 05%	651111-0241	RC05GF241J	81349
R44	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R45	RES FXD COMP 7.5 K 1/8W 05%	651111-0752	RC05GF752J	81349
R46	RES FXD COMP 7.5 K 1/8W 05%	651111-0752	RC05GF752J	81349
R47	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
R48	RES FXD COMP 1 K 1/8W 05%	651111-0102	RC05GF102J	81349
U1	IC OP AMP MOS/FET INPUT	703CA3140	CA3140T	02735

5.2.7. Reader Logic
(Dwg. No. 12307885-01)

The Reader Logic performs the following general functions. (Refer to Section Six for a detailed description.) The circuit accepts the LLC and EC signals from the AGC & Cycle Detector and develops an envelope signal (DC CODE). It determines the direction of the code (forward or reverse), identifies the bits and marker(s), strips out the time information and feeds it in bytes complete with strobes to the TOY Accumulator under control of an Error signal. It develops a 1 PPS UPDATE, for the accumulator which is maintained on-time in forward and develops a DISPLAY START signal. In addition, the XR3 and NASA Reader Logic PCBs accept the serial ONEs from the TOY Accumulator (which are in the IRIG format) and convert them to compatible formats for comparison with their DC CODE signals in the Error Bypass Circuit.

6. STANDARD OPTIONS

6.1. SCOPE OF SECTION

Section Six provides circuit descriptions, logic and schematic diagrams, assembly drawings, and parts lists for the standard options included with your Model 8730.

6.2. OPTIONS INCLUDED

A number of standard options are available for the Model 8730. Standard options, when supplied with the instrument, are described on the following pages.

6.2.1. Coincidence Logic (Option A17)
(Schematic Dwg. No. 12307886-01)

General Description

As shown on Block Diagram Dwg. No. 12307900-02, the Coincidence Option adds Coincidence Logic PCB (A3) and its associated cable, plus front panel switches, S3 through S8, and indicator, DS2, to the Model 8730. In addition, jumper W5 on the Main Board is removed. This option provides an output pulse and an output level at a preset time. The level signal lights a front panel indicator, DS2, at coincidence. This level remains until cleared manually by operating CLEAR switch, S5, or remotely by grounding an external CLEAR input. The preset limit is entered in seconds, minutes, hours and days groups from thumbwheel switches S6, S7, S8. In addition, jumper W5 on the Main Board is removed by operating DISPLAY switch, S3, and LOAD switch, S4, simultaneously. The contents of the coincidence register can be displayed at any time by operating the DISPLAY switch. The selected coincidence output occurs once each day if 000 days are entered.

Specifications

Outputs

A pulse and a continuous level are output at coincidence. The level remains until cleared. Both outputs are positive level, DTL/TTL, compatible signals via rear panel connector J1.

ONE = 5 Vdc ±0.5 Vdc @ 1.2 mA

ZERO = 0 to ±0.1 Vdc, 3.2 mA sink

COIN (M) momentary pulse(s) via (J1,44)

COIN (L) level via (J1,19)

Input

The $\overline{\text{COIN}}$ $\overline{\text{CLEAR}}$ input, to (J1,21), is a ground true signal which clears the coincidence level output. Input may be DTL/TTL, CMOS or contact closure. The source must sink 150 mA.

Coincidence Limit Loading Procedure

Select the seconds (S00 through S59) on the front panel preset thumbwheel switches and operate both the DISPLAY and LOAD switches (up or down as desired). The selected seconds appear in the display. In like manner, load minutes (M00 through M59), hours (H00 through H23), and days (000 through 365/366). The selected times appear in the display when loaded.

If 000 days are entered, coincidence occurs once each day (code time) at the TOD selected. If any other days limit is selected, coincidence will occur once a year (code time).

The stored limit may be viewed at any time by operating the DISPLAY switch.

Circuit Description

Referring to Schematic Dwg. No. 12307886-01, the coincidence limit in days, hours, minutes and seconds is stored in shift register (U1 through U7). The time entered on the front panel preset switches is loaded into the register in groups by the preset control circuit formed from decoder (U9) and gates on (U8) and (U10).

When the front panel DISPLAY switch is pressed, the DISPLAY input to pin 23 goes high opening gate (U10,10) to DISPLAY LOAD pulses, jamming flip-flop (U14,13) into the set state, and setting the Comparator Preset flip-flop ((U21,13) on the Main Board) through (U10,11) and pin 33. Display Control Counter (U13) on the Main Board is enabled. When it counts to ZERO the DISPLAY ZERO signal through pin 24 sets flip-flop (U15,1) which selects the Serial Comparator signal in place of Accumulator Ones through (U17,3), (U18,11 and 34) for input to the Display Shift Register on the Main Board. The contents of the Coincidence Limit Register are displayed in place of the contents of the accumulator.

When the LOAD switch is operated at the same time as the DISPLAY switch, it arms the preset thumbwheel switches. If seconds (S), minutes (M), or hours (H) is selected the appropriate gate on (U8) is opened by the decoded output from (U9) and the selected information is loaded into the Limit Register by the Load Coin signal through pin 28 and (U10,10). If days are selected the 400 line at pin 40 is high and the Load Coin signal through (U8,4) strobes the days into the Limit Register. If OFF is selected, preset is disabled, gate (U10,11) is closed. The contents of the Limit Register can be viewed at any time by pressing only the DISPLAY switch.

The Coincidence Limit stored in the Limit Register is serially compared with the contents of the accumulator once each time-code-frame, when the accumulator contents are sent to the Display (CONTROL FF signal on pin 19 low). This is done in exclusive OR gate (U17,4) on the Main Board which feeds the "not equal to" signal through pin 25 to gate (U21,9). Gate (U21,9) is sampled by the inverse of the SHIFT COMPARATOR signal through pin 30. The output is fed to flip-flops (U14,1) and (U20,13) through gates controlled by flip-flop (U20,1). (These flip-flops are reset, along with counters on (U11) at the start of the transfer sequence.)

Any difference detected between the two data sequences results in the setting of (U14,1) for the first twenty-nine bits which contain the TOD information. At a count of 30 the decoded output from counter (U11) through (U10,4) sets flip-flop (U20,1) which opens gate (U10,3), resulting in the days, provided the limit entered for days is zero. If a ONE bit is present in the days limit, (U20,1) will be cleared through (U21,6) and (U14,1) will serve as the depository for the differences detected in the remainder of the days bits.

NOTE

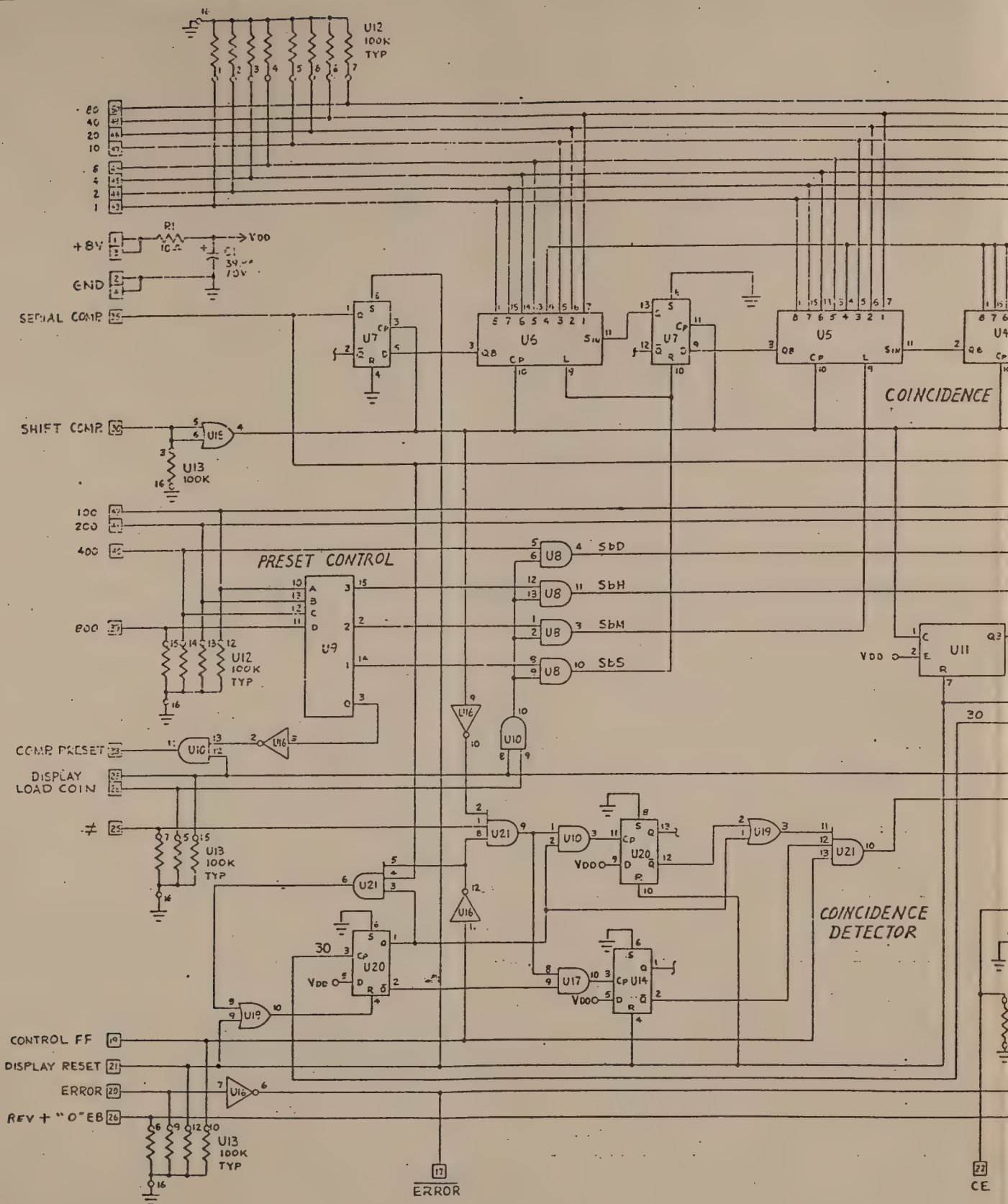
> If the days limit is 000, (U20,1) will remain set after a count of thirty and supply a high through gate (U19,3) to pin 11 of (U21,10) whether or not (U20,13) has been set. This permits a coincidence to occur once a day if 000 days are entered as a limit.

All three inputs to (U21,10) are ONEs at coincidence when the CONTROL FF signal returns high at the end of the compare sequence. The output pulse from (U21,10), which is approximately one time-code-frame wide, is fed through (U17,4), to pin 12 as the COIN (M) output pulse. Gate (U17,4) is open at all times except when operating in forward with Error Bypass and an error is detected.

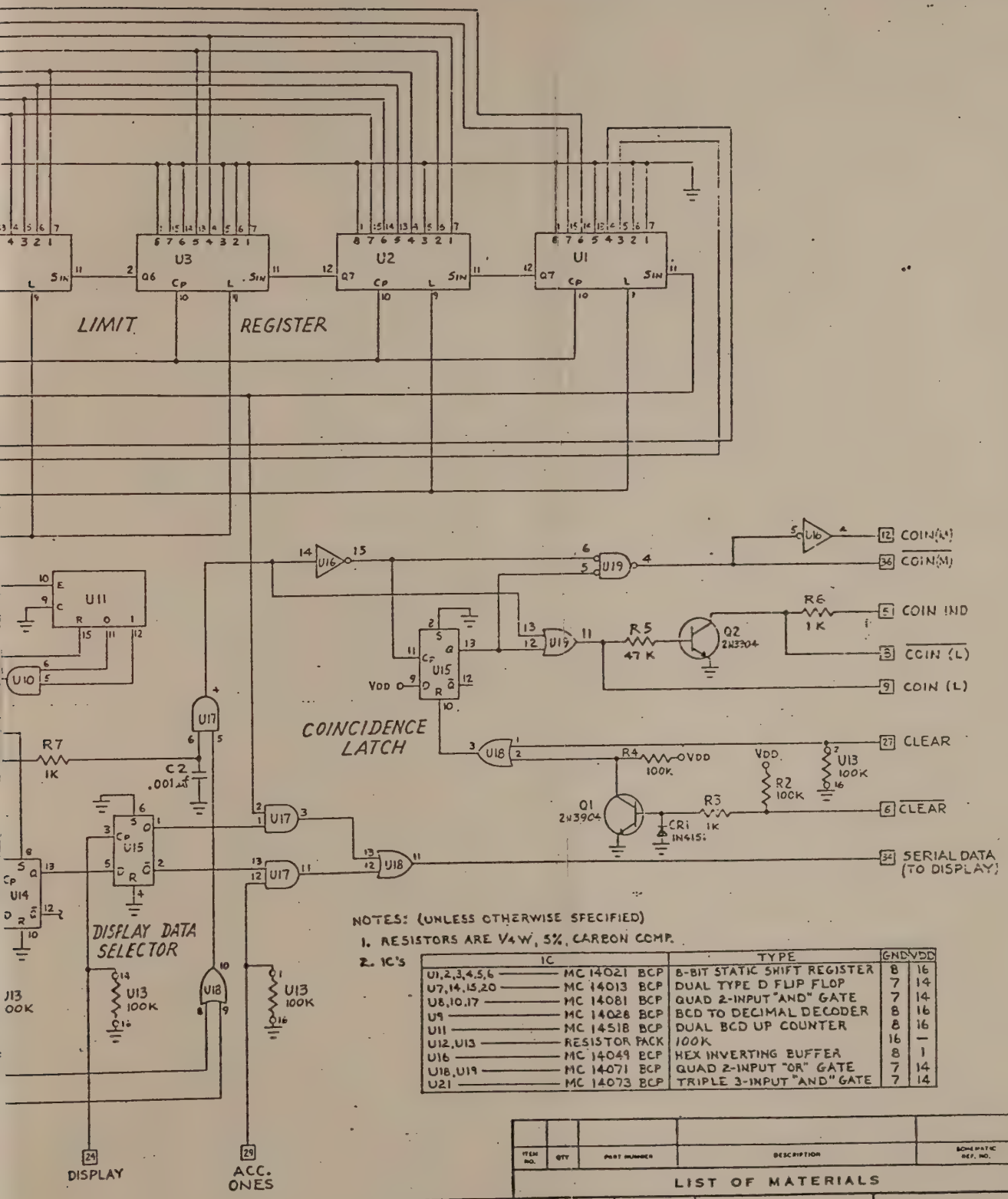
The trailing edge of the coincidence pulse sets flip-flop (U15,13) establishing the COIN (L) level output through (U16,15) and pin 9. Transistor Q2 lights the coincidence indicator through pin 5. Flip-flop (U15,13) stays set until cleared through (U18,3) by a CLEAR input from the front panel push button through pin 27 or by an external CLEAR input through pin 6 and Q1.

ASSEMBLY COINCIDENCE LOGIC OPT A17
ASSEMBLY NUMBER 12807951-1
REFERENCE DESIGNATOR PREFIX 1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
	***** ADD *****			
A1DS2	LED CLR DIFF .200 50 MA	555600-4887	HLMP-0240	28480
A1S3	SW, TOGGLE SPDT ON-OFF-ON MIN	553304-0012	7105SYZQ	09353
-MP1	NUT DRESS 1/4-40 NICK/PLATE	401000-0000	B7099	09353
A1S4	SW, TOGGLE SPDT ON-OFF-ON MIN	553304-0012	7105SYZQ	09353
-MP1	NUT DRESS 1/4-40 NICK/PLATE	401000-0000	B7099	09353
A1S5	SWITCH PSHBTN SPST-NO	553012-0005	39-3	81073
A1S6	SW, THUMBWHEEL L BCD	553101-0005	29078/B	07126
A1S7	SW, THUMBWHEEL L BCD	553101-0005	29078/B	07126
A1S8	SW THUMBWHEEL SEE DRAWING 071858	553101-0011	29-5-84	07126
-MP1	BKT PR SWEND MT BLK MATTE 2900 SER	520835-0041	29-06005-2	07126
-MP2	BKT PR SWEND MT BLK MATTE 2900 SER	520835-0041	29-06005-2	07126
-MP3	SWITCH STRAP PAIR 3 DIGIT	553018-0020	29-57-001-3	07126
-MP4	SWITCH STRAP PAIR 3 DIGIT	553018-0020	29-57-001-3	07126
A1XDS2	LAMP HOLDER	555001-0003	Q-084-3D	03797
A3A4	ASSY. COINCIDENCE LOGIC	10307886-1		24672


U12 100K TYP
80
40
20
10
8
4
2
1
+8V
R1
C1
VDD
END
SERIAL COMP
U7
U6
U5
COINCIDENCE
SHIFT COMP
U19
U13 100K
100
200
400
800
PRESET CONTROL
U9
U8
SbD
SbH
SbM
SbS
U11
VDD
30
COMP PRESET
U16
U10
DISPLAY LOAD COIN
≠
U21
U20
COINCIDENCE DETECTOR
U17
CONTROL FF
DISPLAY RESET
ERROR
REV + "0" EB
ERROR
CE

REV	DESCRIPTION	ENG. NO.	ECO NO.	DATE	APP'D
B	U19-9 WAS TO PIN 19, MOVED TO PIN 21.		TCO 711	9/4/72	C
C	REVISED WIRING IN FRONT OF "COINCIDENCE LATCH" SECTION.	-	11617	11/4/72	
D	C1 WAS 25V.		13795	12-1-72	
E	AUSTRON RELEASE		—	8-7-73	



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE V4W, 5%, CARBON COMP.
2. IC'S

IC		TYPE	GND	VDD
U1,2,3,4,5,6	MC 14021 BCP	8-BIT STATIC SHIFT REGISTER	8	16
U7,14,15,20	MC 14013 BCP	DUAL TYPE D FLIP FLOP	7	14
U8,10,17	MC 14081 BCP	QUAD 2-INPUT "AND" GATE	7	14
U9	MC 14028 BCP	BCD TO DECIMAL DECODER	8	16
U11	MC 14518 BCP	DUAL BCD UP COUNTER	8	16
U12,U13	RESISTOR PACK	100K	16	—
U16	MC 14049 BCP	HEX INVERTING BUFFER	8	1
U18,U19	MC 14071 BCP	QUAD 2-INPUT "OR" GATE	7	14
U21	MC 14073 BCP	TRIPLE 3-INPUT "AND" GATE	7	14

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

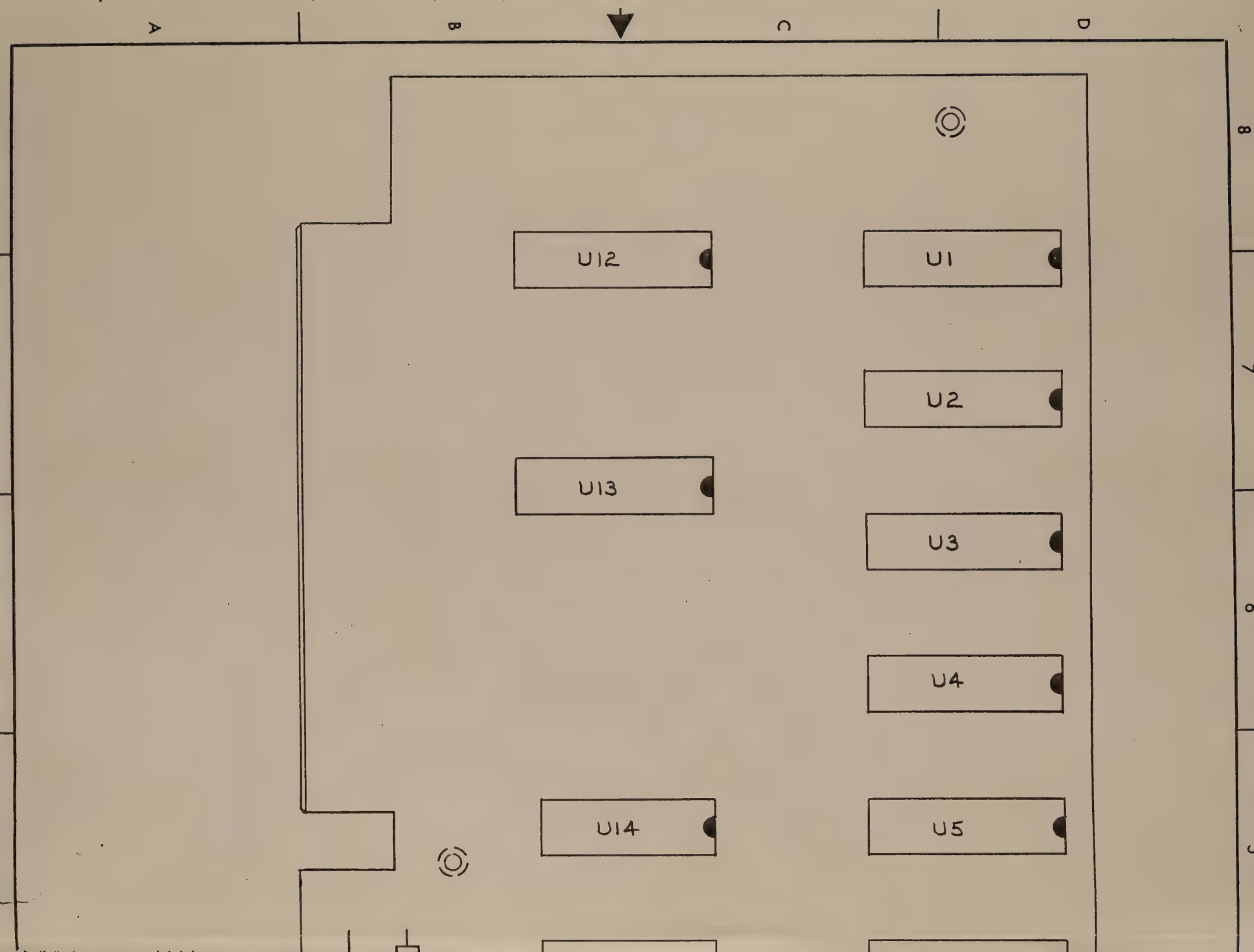
DRAWN A	DATE 10-21-72	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.1 .XX ±.01 .XXX ±.005 ANGLES ±	AUSTRON INC. AUSTIN, TEXAS
CHECK	DATE		CODE IDENT. 24672
ELECT.	DATE		
MECH.	DATE		
PROJECT.	DATE		
QA	DATE		
8730			
USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING
APPLICATION			SH 1 OF 1

COINCIDENCE LOGIC

MATERIAL

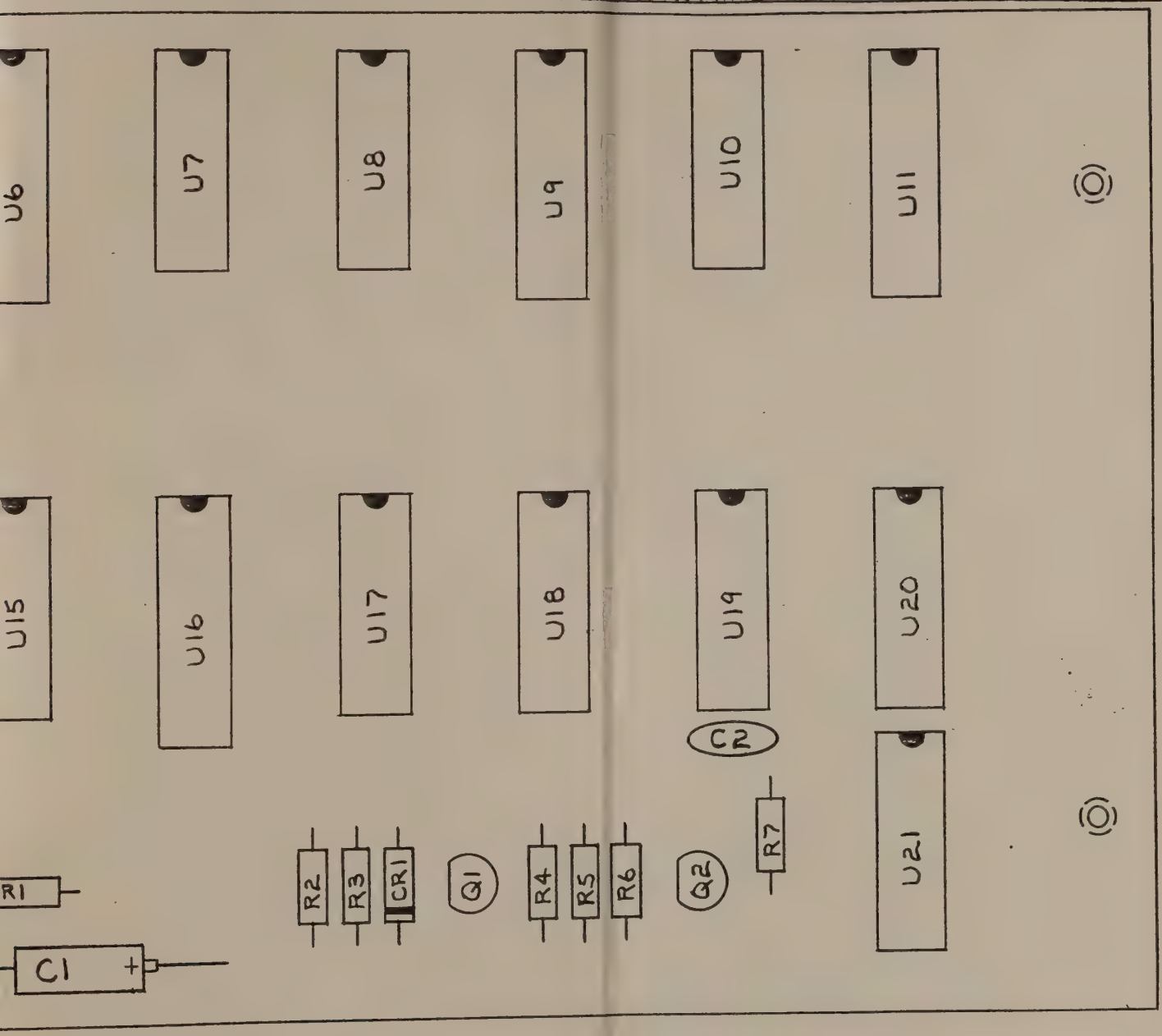
6-6

DRAWING NO.			
REF	SIZE	PART NO.	REV
	D	12307886-1	E


A
B
C
D
U12
U1
U2
U13
U3
U4
U14
U5

D	REVISED P/L 7727 RM	8-15-85	OL
E	REVISED / 8105 RM	10-22-85	OL
F	REVISED / 7955 RM	10-22-85	OL

REV	DESCRIPTION	SER. NO.	ECO NO.	DATE	APP. BY
A					
A1	SPACERS WERE SHOWN WRONG		NFC	3/9	Z
B	CHG'D C1 TO 10V. WAS 20V, & SIZE		13795	11-2-79	RMS BICL.W.
B1	ONE STAND OFF WAS ON TOP SIDE (077-81)		NFC	6/81	RMS
C	DWG NO. WAS 07188601		4837		



ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN T.M.H. 12-6-77	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±, .XX ±, .XXX ±, ANGLES ±	AUSTRON INC. AUSTIN, TEXAS
CHECK	DATE		
ELECT.	DATE		
MECH.	DATE		
PROJECT [illegible] 11/77	DATE		
QA	DATE		

ASSY COINCIDENCE LOGIC

CODE IDENT 24672

USED ON	NEXT ASSY
8730	
APPLICATION	

SCALE	DO NOT SCALE DRAWING	SH 1 OF 2
2:1		

MATERIAL 6-7

DRAWING NO.			
REF	SIZE	PART NO.	REV
	B	10307886-1	F

ASSEMBLY ASSY. COINCIDENCE LOGIC
ASSEMBLY NUMBER 10307886-1
REFERENCE DESIGNATOR PREFIX 1A3A4
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	50V DIO SIG	7011N4151	1N4151	13715
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C2	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
Q1	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q2	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
R1	RES FXD COMP 10 OHM 1/4W 10%	651102-0100	RC07GF100K	81349
R2	RES FXD COMP 100 K 1/4W 10%	651102-0104	RC07GF104K	81349
R3	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R4	RES FXD COMP 100 K 1/4W 10%	651102-0104	RC07GF104K	81349
R5	RES FXD COMP 47 K 1/4W 10%	651102-0473	RC07GF473K	81349
R6	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R7	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
U1	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U2	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U3	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U4	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U5	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U6	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713
U7	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U8	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U9	IC CMOS BCD-DEC DCD	703MC14028BP	MC14028BCP	04713
U10	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U11	IC CMOS DUAL BCD UP CNTR F>2	703MC14518BP	MC14518BCP	04713
U12	RES FXD DIPNET 14P 100 K 1.75W 2%	654013-0104	314A104	01121
U13	RES FXD DIPNET 14P 100 K 1.75W 2%	654013-0104	314A104	01121
U14	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U15	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U16	IC CMOS HEX INV/BUFF	703MC14049BP	MC14049UBCP	04713
U18	IC CMOS 4 2IN OR 14DIP	703MC14071BP	MC14071BCP	04713
U19	IC CMOS 4 2IN OR 14DIP	703MC14071BP	MC14071BCP	04713
U20	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U20	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U21	IC CMOS 3*3IN AND	703CD4073BE	CD4073BE	02735

6.2.2. IRIG A/B Time Code (Option C41) (Schematic Dwg. No. 12307885-01)

General Description

As shown on Block Diagram Dwg. No. 12307900-02, the IRIG A/B Time Code Option adds IRIG A/B Reader Logic PCB (A3) connected via a flat cable to the Main Board. The IRIG A/B Reader Logic accepts the LLC and EC outputs from the AGC & Cycle Detector. (The input code may have the IRIG A or B format as selected by a slide switch (S1) on the rear panel of the Model 8730.) Based on these inputs, it develops an envelope (DC CODE), determines the direction of the code (forward or reverse), identifies the bits and markers, strips out the time information and feeds this (in bytes complete with strobes) to the TOY Accumulator under control of an Error Bypass signal. The circuit develops a 1 PPS UPDATE, three PULSE Rates, the DISPLAY START signal and the ACCUMULATOR SHIFT signal. It also provides an extension to the TOY Accumulator and shift register (for tenths-of-seconds) when reading the IRIG A Code.

Circuit Description

Referring to Schematic Dwg. No. 12307885-02, the Envelope and Code Direction Detectors are shown at the upper left.

The Envelope Detector, formed from flip-flops (U20,1 and 13), reconstructs the DC CODE from the LLC and EC input signals. The Envelope (or its complement) is fed to the Main Board (where it is output through a buffer); to the Code Direction Detector; to the Data Register (which accumulates data bytes); to the Mark Detector and through ((U13,4) or C2, R17 and (U1)) to (U3) as the Z-COUNTER RESET.

The Code Direction Detector is formed from counter (U5), flip-flops on (U9) and (U19) plus gates (U6,10), (U13,10 and 11) and inverters (U12) and (U18). The circuit accepts LLC, EC, Envelope and Double Mark signals and from these determines the direction of the input code. The circuit does this by counting the number of small cycles following the second mark in the double mark at the beginning of the code frame. If the number of small cycles is less than four, the code is assumed to be forward. If four or greater, it is assumed to be reverse.

The REV and/or FWD outputs from (U19,12 and 13) are fed to gates (U2,10) and (U10,3) (which select the EC edge to be counted by Z-Counter (U3)); to four-bit selector (U1) (which selects Z-Counter Reset, Data Register Clock, Mark Detector Clock and X-Counter Reset Strobe)); to the Data Register; to the Display Start circuit; to the X-and Y-Counter Reset circuits and to the 0.1 Second Accumulator. The Z-Counter (U3) is a decade which is clocked at the carrier (EC) rate. The circuit develops the ACCUMULATOR SHIFT signal plus sampling signals for bit and marker identification. The output at (U3,12), a square wave at the code bit rate, (100 ppf) clocks the X-Counter (decade (U4)). The 10 ppf square wave output from (U4,12), in turn, clocks Y-Counter (U17). These counters are synchronized with the input code frame. The X- and Y-Counters are synchronized by the Mark and Double Mark outputs from the Mark Detector and gate (U11,3). They develop pulse rates, control loading of the Data Register and steer data bytes into the TOY Accumulator.

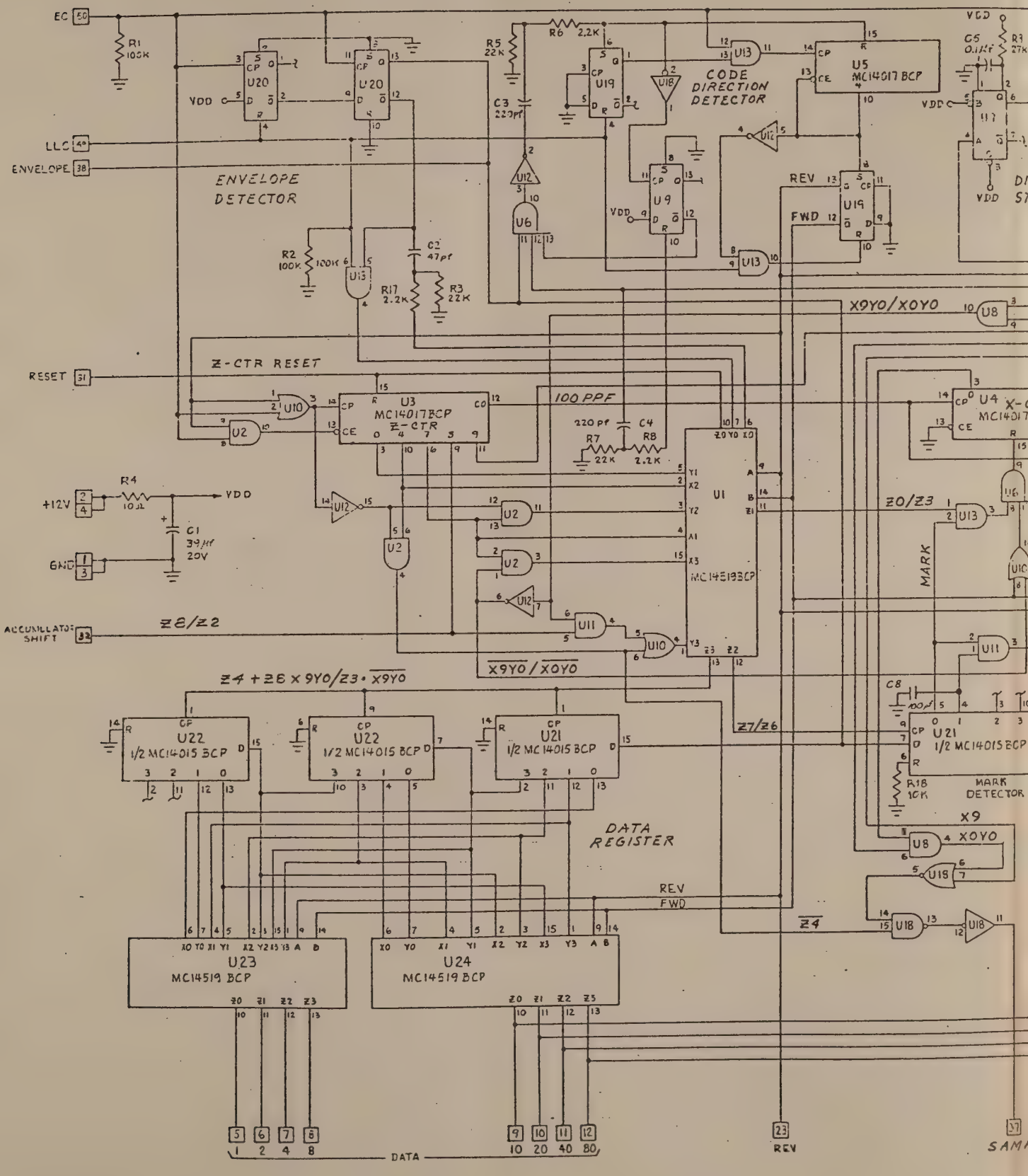
The Data Register (formed from shift registers on (U21) and (U22) plus selectors (U23), (U24)) accepts the envelope signal at the serial input to the shift register. The shift register clock from (U1,3) is timed to occur when the Envelope is low for a ZERO bit and high for a ONE bit thus identifying the code time data bits as they are loaded. An extra shift is generated in forward and one less in reverse during the YØ period to maintain a consistent location of bits at the parallel outputs from the shift register. The order of data bits is maintained constant (regardless of code direction) by selectors (U23) and (U24) under control of the FWD and REV signals.

The data outputs are fed to the TOY Accumulator where they are loaded under the control of strobe signals generated at the outputs from three-state buffers on (U16). (See upper right-hand area of the schematic.) The strobes are generated near the end of each of the first five Y-times in the code frame (YØ through Y4) whenever the ERROR signal is high. (Refer to the Error Bypass description in Section Five.) The strobe pulses are developed by gate (U6,6) through inverter (U18,3) and each strobe is selected by the outputs from Y-Time Decoder (U15) which is controlled by the BCD outputs from Y-Counter (U17).

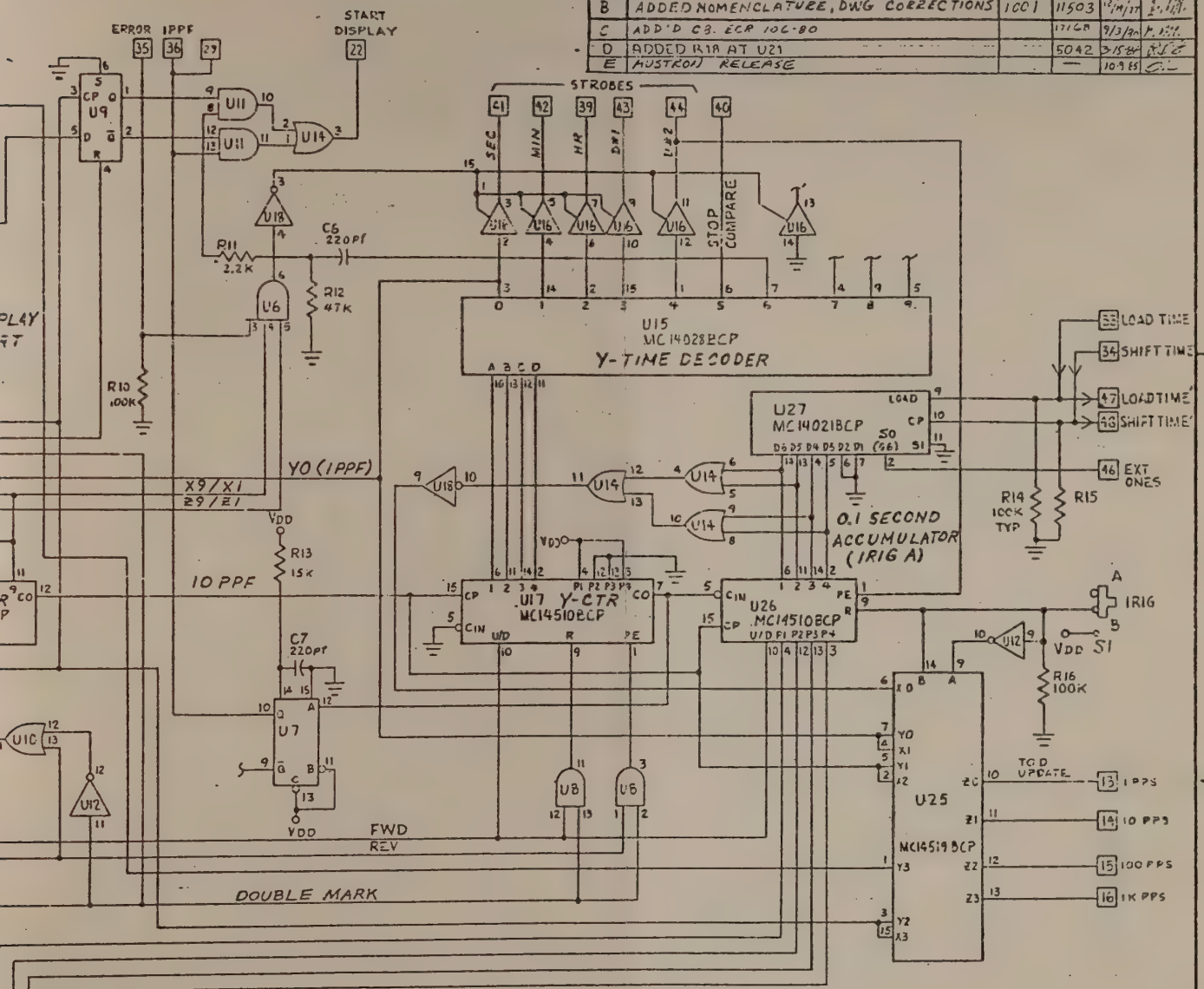
The 0.1 Second Accumulator, consisting of decade (U26) and shift register (U27), extends the TOY Accumulator on the Main Board to include tenths-of-seconds when the IRIG A Time Code is being read. Tenths-of-seconds are included in the Serial ONEs out of the shift register for use by the Error Bypass circuit. Code switch, S1, enables (U26) and selects 1 PPS (TOD) UPDATE and pulse rates through selector (U25).

The SAMPLE and 1 PPF signals used by Error Bypass are developed by gates (U8,4), (U18,5 and 13) and one-shot (U7,10), respectively. SAMPLE is a gated Z4 signal which is present for active code data bits in forward. The 1 PPF signal is derived from the carry out of the Y-Counter.

The 1 PPF signal is also gated out through (U11,11) and (U14,3) as the START DISPLAY signal at low code rates. For high code rates in forward the DISPLAY START circuit, formed from one-shot (U7,6) and flip-flop (U9,1), selects the differentiated leading edge of Y6 through C6, R1, (U11,10), (U14,3) as the START DISPLAY signal.


EC
LLC
ENVELOPE
ENVELOPE DETECTOR
CODE DIRECTION DETECTOR
RESET
Z-CTR RESET
MC14017BCP Z-CTR
100 PPF
MC14519BCP
X9Y0/X0Y0
Z0/Z3
MARK
MARK DETECTOR
Z8/Z2
Z4 + Z8 X 9Y0/Z3 · X9Y0
Z7/Z6
DATA REGISTER
REV
FWD
DATA
+12V
GND
ACCUMULATOR SHIFT
1 2 4 8
10 20 40 80

REVISIONS					
REV	DESCRIPTION	ENG. NO.	ECO NO	DATE	APP. BY
B	ADDED NOMENCLATURE, DWG CORRECTIONS	1001	11503	12/14/77	
C	ADD'D C8. ECR 10C-80		11768	9/3/78	
D	ADDED R18 AT U21		5042	3/15/84	
E	AUSTRON RELEASE		—	10-9-85	



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE 1/4 W, 5%, CARBON COMP.

2. IC's

IC		TYPE	GND	VDD
U1,23,24,25	MC 14519 BCP	4-BIT AND/OR SELECTOR	8	16
U2,8,11,13	MC 14081 BCP	QUAD 2-INPUT "AND" GATE	7	14
U3,4,5	MC 14017 BCP	DECADE COUNTER/DIVIDER	8	16
U6	MC 14073 BCP	TRIPLE 3-INPUT "AND" GATE	7	14
U7	MC 14528 BCP	DUAL RETRIGGERABLE ONE-SHOT	8	16
U9,19,20	MC 14013 BCP	DUAL TYPE D FLIP-FLOP	7	14
U10,14	MC 14071 BCP	QUAD 2-INPUT "OR" GATE	7	14
U12	MC 14049 BCP	HEX INVERTING BUFFER	8	1
U15	MC 14028 BCP	BCD TO DECIMAL DECODER	8	16
U16	MC 14503 BCP	HEX 3-STATE BUFFER	8	16
U17,26	MC 14510 BCP	BCD UP/DOWN COUNTER	8	16
U18	MC 14572 BCP	HEX GATE	8	16
U21,22	MC 14015 BCP	DUAL 4-BIT STATIC S.R.	8	16
U27	MC 14021 BCP	8-BIT STATIC SHIFT REGISTER	8	16

ACC. ONES → 17
ONES → 19
N/C ← TIME DISPLAY 18
N/C ← DISPLAY CLOCK 20
N/C ← XR3 (250HZ) 21
N/C ← DAYS RESET 24

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN JE 8-12-77	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±, .XX ±, .XXX ANGLES ±	AUSTRON INC. AUSTIN, TEXAS
CHECK	DATE		
ELECT.	DATE		
MECH.	DATE		
PROJECT 11/17	DATE		
QA	DATE		
5730 USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING
APPLICATION			SH 1 OF 1

IRIG A/B READER LOGIC

CODE IDENT. 24672

MATERIAL 6-12

DRAWING NO.

REF	SIZE	PART NO.	REV
7	D	12307885-1	E

ASSEMBLY PCB ASSY IRIG A/B READER LOGIC
ASSEMBLY NUMBER 10307885-1
REFERENCE DESIGNATOR PREFIX 1A3A3
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	39 UF 20V 10 CAP TANT	608116-0396	150D396X9020R2	56289
C2	47 PF 500V 5 CAP DIP MICA	603000-0470	DM15-470J	02799
C3	220 PF 500V 5 CAP DIP MICA	603000-0221	CM05FD221J03	09023
C4	220 PF 500V 5 CAP DIP MICA	603000-0221	CM05FD221J03	09023
C5	.1 UF 50V 20 CAP CER DP	601009-0104	2C37Z5U104M050B	56289
C6	220 PF 500V 5 CAP DIP MICA	603000-0221	CM05FD221J03	09023
C7	220 PF 500V 5 CAP DIP MICA	603000-0221	CM05FD221J03	09023
C8	CAP CERA RDL COG 100 PF 200V 5%	605110-0101	C320C101J2G5CA	31433
R1	RES FXD COMP 100 K 1/4W 10%	651102-0104	RC07GF104K	81349
R2	RES FXD COMP 100 K 1/4W 10%	651102-0104	RC07GF104K	81349
R3	RES FXD COMP 22 K 1/4W 10%	651102-0223	RC07GF223K	81349
R4	RES FXD COMP 10 OHM 1/4W 10%	651102-0100	RC07GF100K	81349
R5	RES FXD COMP 22 K 1/4W 10%	651102-0223	RC07GF223K	81349
R6	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R7	RES FXD COMP 22 K 1/4W 10%	651102-0223	RC07GF223K	81349
R8	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R9	RES FXD COMP 27 K 1/4W 10%	651102-0273	RC07GF273K	81349
R10	RES FXD COMP 100 K 1/4W 10%	651102-0104	RC07GF104K	81349
R11	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R12	RES FXD COMP 47 K 1/4W 10%	651102-0473	RC07GF473K	81349
R13	RES FXD COMP 15 K 1/4W 10%	651102-0153	RC07GF153K	81349
R16	RES FXD COMP 100 K 1/4W 10%	651102-0104	RC07GF104K	81349
R17	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
S1	SW, SLIDE DPDT RT. ANGL	553007-0002	GI-152-DPDT	79727
U1	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U2	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U3	IC CMOS DEC CNTR 5STAGE JOH	703MC14017BP	MC14017BCP	04713
U4	IC CMOS DEC CNTR 5STAGE JOH	703MC14017BP	MC14017BCP	04713
U5	IC CMOS DEC CNTR 5STAGE JOH	703MC14017BP	MC14017BCP	04713
U6	IC CMOS 3*3IN AND	703CD4073BE	CD4073BE	02735
U7	IC CMOS DUAL MONOSTBL MULTI	703MC14528BP	MC14528BCP	04713
U8	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U9	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713

ASSEMBLY PCB ASSY IRIG A/B READER LOGIC (CONT)
ASSEMBLY NUMBER 10307885-1
REFERENCE DESIGNATOR PREFIX 1A3A3
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U10	IC CMOS 4 2IN OR 14DIP	703MC14071BP	MC14071BCP	04713
U11	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U12	IC CMOS HEX INV/BUFF	703MC14049BP	MC14049UBCP	04713
U13	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U14	IC CMOS 4 2IN OR 14DIP	703MC14071BP	MC14071BCP	04713
U15	IC CMOS BCD-DEC DCD	703MC14028BP	MC14028BCP	04713
U16	IC CMOS HEX DRIVER TRI STATE OUT	703MC14503BP	MC14503BCP	04713
U17	IC CMOS BCD-PRST UP-DWN CNTR	703MC14510BP	MC14510BCP	04713
U18	IC CMOS	703MC14572	MC14572	04713
U19	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U20	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U21	IC CMOS 2*4BIT STATIC SR 16	703MC14015BP	MC14015BCP	04713
U22	IC CMOS 2*4BIT STATIC SR 16	703MC14015BP	MC14015BCP	04713
U23	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U24	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U25	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U26	IC CMOS BCD-PRST UP-DWN CNTR	703MC14510BP	MC14510BCP	04713
U27	IC CMOS 8-BIT STATIC SHIFT REGISTER	703MC14021BC	MC14021BCB	04713

6.2.3. XR3 250 Hz/1 kHz Time Code (Option C47) (Schematic Dwg. No. 12308142-01)

As noted on the Model 8730 Block Diagram Dwg. No. 12307900-02, the XR3 250 Hz/1 kHz Reader Logic PCB (Assembly Dwg. No. 10308142-01) is substituted for the IRIG A/B Reader Logic PCB in location A3. It is connected via a flat cable to the Main Board. The XR3 Reader Logic accepts the LLC and EC outputs from the AGC and Cycle Detector. (The input code may have a 250 Hz or 1 kHz carrier as selected by switch (S1) on the rear panel of the Model 8730.) Based on these inputs, the Reader Logic develops an envelope (DC CODE), determines the direction of the code (forward or reverse), identifies the bits and markers; then strips out the time information and feeds it in hours, minutes and seconds bytes to the TOD section of the TOY Accumulator. Days are jammed to ZERO. The above events are controlled by the Error Bypass circuitry which compares the incoming code with an equivalent XR3 format derived from the serial output from the TOY Accumulator when operating in forward.

In addition, the XR3 Reader Logic develops a 1 PPS UPDATE and the DISPLAY START signal.

Circuit Description

Referring to Schematic Dwg. No. 12308142-01, the Envelope and Code Direction Detectors are shown at the upper left.

The Envelope Detector formed from flip-flops on (U13) reconstructs the DC CODE from the LLC and EC input signals. The Envelope signal from (U13,13) is fed to the Main Board (where it is output through a buffer), to the Code Direction Detector, to the Data Register and to the Mark Detector. The complement signal from (U13,12) is fed through (U15,10) or C2/R4, (as selected by switch (U11,13)) to the pre-divider and Z-Counter as the SYNC INPUT signal.

The Code Direction Detector (formed from counters on (U16), flip-flops on (U5) plus gates on (U15) and (U18)) accepts the envelope, 250 PPS and MARK signals and from these determines the direction of the input code. It does this by counting the number of small cycles (250 PPS) following the MARK at the end of the Code. If the number is less than eight, the code is assumed to be forward. If equal to or greater than eight, it is assumed to be reverse.

The FWD and REV outputs from (U15,13 and 12) are fed as control inputs to switches on (U4), (U11), (U27) and (U28) which select Z-COUNTER and MARK signals, DATA STROBE and PRE-DIVIDER/Z-COUNTER SYNC signals, and the data bit order, respectively. The FWD signal is also fed to gate (U15,4) which enables preset of the Z-Counter to ONE in forward when reading an XR3 (250 Hz) Code. The REV signal is also fed to flip-flop (U6,13) adding the Y4X4Z6 strobe to the normal Z4 Data Register Clock signals in reverse.

The pre-divider formed from flip-flops on (U12) divides the EC by four when reading the XR3 (1 kHz) Code. The Z-Counter (U2) is a decade which is clocked at 250 pps (EC or EC/4). It develops the 25 pps X-Counter update. The BCD outputs are decoded in (U3) developing the ACCUMULATOR SHIFT signal plus sampling signals for bit and marker identification and for generation of Data Strobes.

The X-Counter (U20) clocks the Y-Counter (U21) on the trailing edge of the X4 output through one-shot (U19,10). The carry from (U19,10) also clears (U20) through gate (U18,11) thus making it a scale-of-five counter. Counter (U21) is also a scale-of-five. It is cleared on the trailing edge of Y4 through inverter (U7,3), C8, R13 and gate (U18,10). Both counters are synchronized by the differentiated MARK signal at the end of the frame.

The X-and Y-Counters output decoded signals which steer Z6 pulses through gates on (U9) and (U10) to establish Forward and Reverse Data Strobes. In the Forward Direction, the Z6 pulses are ANDed with the error output from the Error Bypass circuit on the Main Board. The selection between forward and reverse strobes is made by switches on (U11). The Data Strobes load Time Data Bytes into the TOD section of the TOY Accumulator on the Main Board. (Days are jammed to ZERO.)

The Data Register is formed from two 4-bit shift registers on (U29) connected in tandem plus selectors on (U27) and (U28). The shift register accepts the envelope signal at the serial input and is clocked by Z6 in forward and Z4 in reverse. The clock signal is timed to occur when the envelope is low for a ZERO bit and high for a ONE bit thus identifying the code time data bits as they are loaded. The order of data bits in each output byte is maintained constant regardless of code direction by the selectors on (U27) and (U28) which are controlled by the FWD and REV signals.

The Time Data outputs are fed to the TOD section of the TOY Accumulator where they are loaded by the Data Strobe signals. These strobes are controlled by Error Bypass in the forward direction. There is no transfer unless the selected number of consecutive errors occur.

The Error Bypass circuit on the Main Board compares the bits in the envelope signal derived from the input code with a reconstructed serial ONEs data stream representing the current TOD in the TOY Accumulator. This ONEs signal is derived from the accumulator ONEs data (which is in the IRIG B format) when it is fed to the display circuitry once each code frame. This is done by the code conversion logic shown at the bottom of the schematic. Left/right shift register (U30) is fed the accumulator ONEs data in the shift right mode under control of the display clock when these data are being fed to the display. Counters on (U33) and (U31) along with gates on (U22) and (U23) suppress the loading of extraneous bits thus establishing the contiguous bit configuration of the XR3 format.

When all twenty TOD bits are loaded, the counter is frozen by the output from (U24,4) and the shift register is placed in the shift left mode under control of the accumulator shift output from (U15,3). Left/right shift and the shift register clock are selected by flip-flop (U26,1) and switches on (U1).

The SAMPLE and 1 PPF signals are used by the Error Bypass circuit in forward. SAMPLE is a Z6 signal and 1 PPF is the differentiated trailing edge of Y4 at low speeds and Y4X0Z6 at high code speeds. Code speed is detected by the display start circuit formed from one-shot (U19,6), flip-flop (U6,13) and switches on (U17). The 1 PPF signal is also output through pin 22 as the START DISPLAY signal.

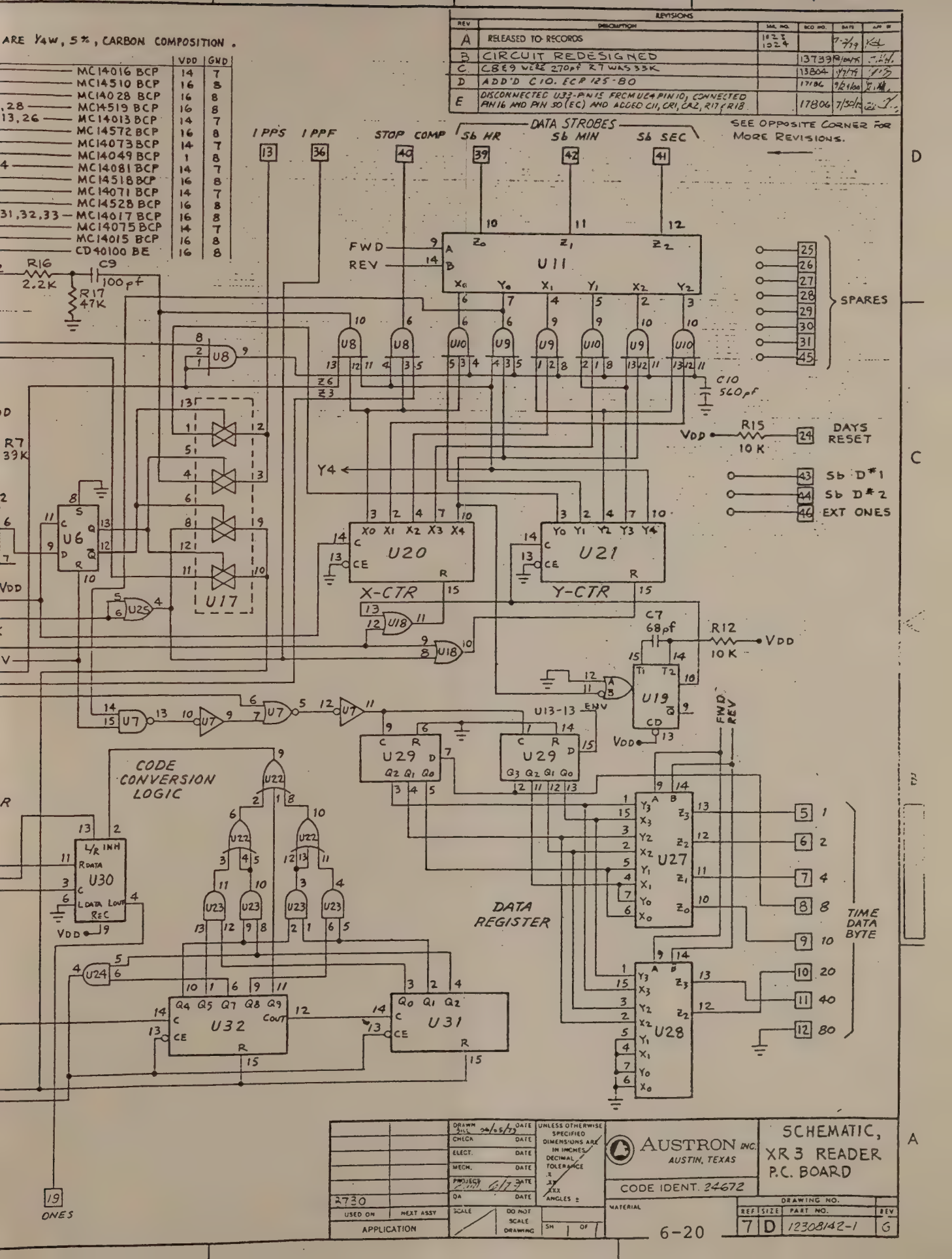
ASSEMBLY OPTION (C47) SW.SEL XR3-1KHZ/250HZ
ASSEMBLY NUMBER 12808142-3
REFERENCE DESIGNATOR PREFIX 1A3
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
	***** DELETE ****			
A3	PCB ASSY IRIG A/B READER LOGIC	10307885-1		24672
	***** ADD *****			
A3	PCB ASSY, XR3 READER LOGIC	10308142-1		24672

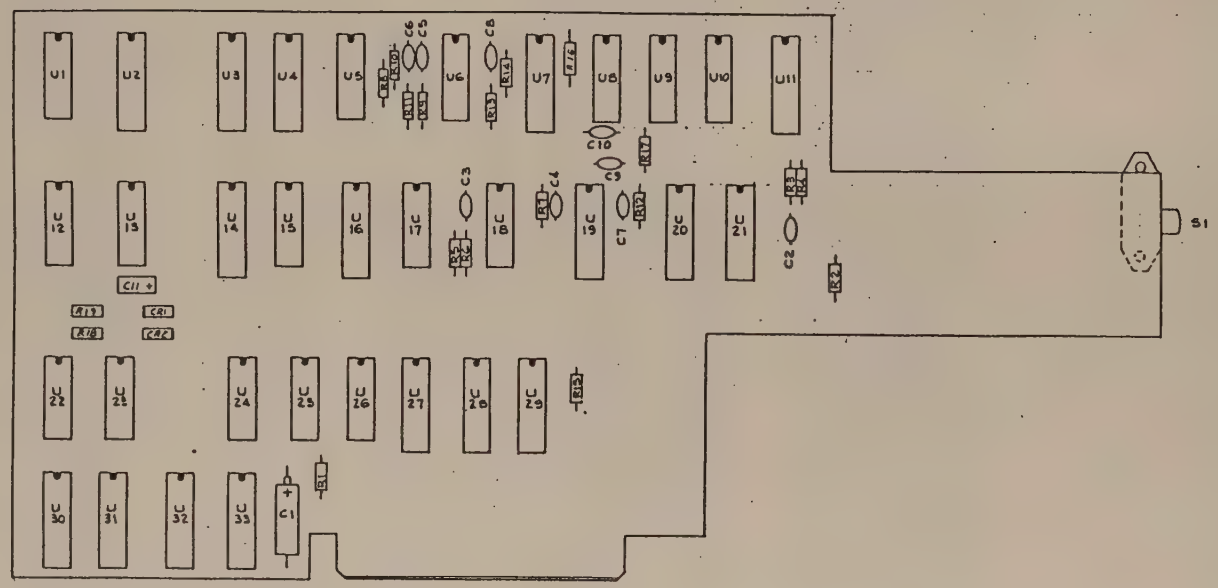
ECR 2011-32					
	E	CHG'D U24 FROM "OR" GATE TO "AND" GATE.			
	F	R19 WAS R17 (WRITTEN TWICE).			
	G	DWG NO. WAS 08114201, ECO 4237			

NOTES
1. RESISTORS
2. INT. CKT.
U1, 17 —
U2 —
U3 —
U4, 11, 2
U5, 6, 17
U7 —
U8, 9, 10
U14 —
U15, 23,
U16 —
U18, 25
U19 —
U20, 21
U22 —
U29 —
U30 —

XR3 (250 HZ) ENV
21 38
REV 23
S1 XR3 1kHz 250Hz
ENVELOPE DETECTOR
VDD
EC 50
LLC 49
ERROR 35
U13 U13
C2 47pf
R3 22K
R4 2.2K
U15
U11
R2 100K
PRE DIVIDER
U12 U12
16
DISPLAY CK 20
+8V 2 4
GND 1 3
R1 10Ω
C1 39μf 20V
U1
U26
ACC ONES 17
DISPLAY TIME 18
U26
CR1 IN4151
LOAD TIME 33
SHIFT TIME 34
START DISPLAY 22
C11 1μF
CR2 IN4151
R18 100K
R19 10CK
C3 220pf
R5 22K
R6 2.2K
250 PPS
U18 U16 U16
CODE DIRECTION DETECTOR
U15 U5 U5
U18
U14
REV
FWD
U15 VDD
U2
PE P1 U/D P2 P3 P4 R CIN COUT
C Q1 Q2 Q3 Q4
Z-CTR
U3
A B C D
Z3 Z7 Z6 Z4
U14
U4
X0 Y0 X1 Y1 X2 Y2 X3 Y3
Z0 Z1 Z2 Z3
FWD Z3/REV Z7
Y4 A21-10
25 PPS
VDD
U19
R14 47K
C8 100pf
U7
MARK ENV
U29-15
Z6
Z3
FWD Z6/REV Z
R10 22K
R11 22K
R8 2.2K
R9 22K
MARK DETECT
C5 220pf
C6 220pf
U6
U33
U24 U25 U24 U25
U14
U25 U25
C4 0.1μf
32 ACC. SHIFT
37 SAMPLE
47 LOAD TIME
45 SHIFT TIME


REVISIONS
REV | DESCRIPTION | ENG. NO. | ECO NO. | DATE | APP'D
A | RELEASED TO RECORDS | 1021 1024 | | 7-7-79 | KL
B | CIRCUIT REDESIGNED | | 13739 | 10/1/79 | KL
C | CB69 WERE 270pF R7 WAS 33K | | 13804 | 12/7/79 | KL
D | ADD'D C10. ECR 125-80 | | 17186 | 9/21/80 | K.M.
E | DISCONNECTED U33-PIN 15 FROM U24 PIN 10, CONNECTED PIN 16 AND PIN 30 (EC) AND ADDED C11, CR1, CR2, R17 & R18. | | 17806 | 7/30/82 | K.J.
SEE OPPOSITE CORNER FOR MORE REVISIONS.
ARE 1/4W, 5%, CARBON COMPOSITION.
MC14016 BCP 14 7
MC14510 BCP 16 8
MC14028 BCP 16 8
MC14519 BCP 16 8
MC14013 BCP 14 7
MC14572 BCP 16 8
MC14073 BCP 14 7
MC14049 BCP 1 8
MC14081 BCP 14 7
MC14518 BCP 16 8
MC14071 BCP 14 7
MC14528 BCP 16 8
MC14017 BCP 16 8
MC14075 BCP 14 7
MC14015 BCP 16 8
CD40100 BE 16 8
1 PPS
1 PPF
STOP COMP
DATA STROBES
Sb HR
Sb MIN
Sb SEC
FWD
REV
U11
SPARES
R16 2.2K
C9 100pF
R17 47K
C10 560pF
R15 10K
DAYS RESET
Sb D*1
Sb D*2
EXT ONES
U6
U17
U25
U20
X-CTR
U21
Y-CTR
U18
C7 68pF
R12 10K
U19
U13-13 ENV
FWD REV
U29
CODE CONVERSION LOGIC
U22
U23
U30
L/R INH
RDATA
LDATA LOUT REC
U24
U32
U31
DATA REGISTER
U27
U28
TIME DATA BYTE
ONES
SCHEMATIC, XR 3 READER P.C. BOARD
AUSTRON INC. AUSTIN, TEXAS
CODE IDENT. 24672
DRAWING NO. 12308142-1
REF 7 SIZE D REV G
2730
APPLICATION
6-20

REV	DESCRIPTION			
B	CIRCUIT REDESIGN		11739	7-7-81
C	CA1C9 WERE 330 PF R1 WAS 33K		13640	11/1/81
C1	CORRECTED U NUMBERS		NRC	11/17/81
D	ADD'D C10		11986	4/14/82
E	ADDED C11, CR1, CR2, R17 & R18		12811	7/1/82
F	DUPLICATE R17'S. CORR. DRAFT. ERROR		11964	7/19/82
G	DWG. NO. WAS 08119201	—	14837	10/15/82
H				



LIST OF MATERIALS

AUSTRON INC
AUSTIN, TEXAS

CODE IDENT 24672

P.C. ASSY
XR3
READER

B130

ASSEMBLY PCB ASSY
ASSEMBLY NUMBER 10308142-1
REFERENCE DESIGNATOR PREFIX 1A3A3
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	39 UF 20V 10 CAP TANT	608116-0396	150D396X9020R2	56289
C2	47 PF 100V 5 CAP CER DP	601110-0470	C312C470J1G5	96733
C3	CAP CERA RDL COG 220 PF 100V 5%	601110-0221	CN15A221J261	71590
C4	.1 UF 10V DISC CERAMIC	601007-0104	UK10-104	71590
C5	CAP CERA RDL COG 220 PF 100V 5%	601110-0221	CN15A221J261	71590
C6	CAP CERA RDL COG 220 PF 100V 5%	601110-0221	CN15A221J261	71590
C7	68 PF 100V 5 CAP CER DP	601110-0680	C312C680J1G5	96733
C8	CAP CERA RDL COG 100 PF 200V 5%	605110-0101	C320C101J2G5CA	31433
C9	CAP CERA RDL COG 100 PF 200V 5%	605110-0101	C320C101J2G5CA	31433
C10	CAP CERA RDL COG 560 PF 100V 5%	601110-0561	CN20A561J242	71590
R1	RES FXD COMP 10 OHM 1/4W 10%	651102-0100	RC07GF100K	81349
R2	RES FXD COMP 100 K 1/4W 10%	651102-0104	RC07GF104K	81349
R3	RES FXD COMP 22 K 1/4W 10%	651102-0223	RC07GF223K	81349
R4	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R5	RES FXD COMP 22 K 1/4W 10%	651102-0223	RC07GF223K	81349
R6	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R7	RES FXD COMP 39 K 1/4W 10%	651102-0393	RC07GF393K	81349
R8	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R9	RES FXD COMP 22 K 1/4W 10%	651102-0223	RC07GF223K	81349
R10	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R11	RES FXD COMP 22 K 1/4W 10%	651102-0223	RC07GF223K	81349
R12	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R13	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R14	RES FXD COMP 47 K 1/4W 10%	651102-0473	RC07GF473K	81349
R15	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R16	RES FXD COMP 2.2 K 1/4W 10%	651102-0222	RC07GF222K	81349
R17	RES FXD COMP 47 K 1/4W 10%	651102-0473	RC07GF473K	81349
S1	SW, SLIDE DPDT RT. ANGL	553007-0002	GI-152-DPDT	79727
U2	IC CMOS BCD-PRST UP-DWN CNTR	703MC14510BP	MC14510BCP	04713
U3	IC CMOS BCD-DEC DCD	703MC14028BP	MC14028BCP	04713
U4	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U5	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U6	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713

ASSEMBLY PCB ASSY (CONT)
ASSEMBLY NUMBER 10308142-1
REFERENCE DESIGNATOR PREFIX 1A3A3
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U7	IC CMOS HEX INVERTER	703MC14572BP	MC14572BCP	04713
U8	IC CMOS 3*3IN AND	703CD4073BE	CD4073BE	02735
U9	IC CMOS 3*3IN AND	703CD4073BE	CD4073BE	02735
U10	IC CMOS 3*3IN AND	703CD4073BE	CD4073BE	02735
U11	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U12	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U13	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U14	IC CMOS HEX INV/BUFF	703MC14049BP	MC14049UBCP	04713
U15	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U16	IC CMOS DUAL BCD UP CNTR F>2	703MC14518BP	MC14518BCP	04713
U18	IC CMOS 4 2IN OR 14DIP	703MC14071BP	MC14071BCP	04713
U19	IC CMOS DUAL MONOSTBL MULTI	703MC14528BP	MC14528BCP	04713
U20	IC CMOS DEC CNTR 5STAGE JOH	703MC14017BP	MC14017BCP	04713
U21	IC CMOS DEC CNTR 5STAGE JOH	703MC14017BP	MC14017BCP	04713
U22	IC CMOS 3X3 IN	703MM4075B	SD-116245	04713
U23	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U24	IC CMOS 4-2IN AND 14DIP	703MC14081BP	MC14081BCP	04713
U25	IC CMOS 4 2IN OR 14DIP	703MC14071BP	MC14071BCP	04713
U26	IC CMOS DUAL D F/F,IN D,CLK	703MC14013BP	MC14013BCP	04713
U27	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U28	IC CMOS 4BIT AND/OR SELECTR	703MC14519BP	MC14519BCP	04713
U29	IC CMOS 2*4BIT STATIC SR 16	703MC14015BP	MC14015BCP	04713
U30	ICCMOS 32 BIT 4R SHIFT REGISTER	703CD40100BE	CD40100BE	02735
U31	IC CMOS DEC CNTR 5STAGE JOH	703MC14017BP	MC14017BCP	04713
U32	IC CMOS DEC CNTR 5STAGE JOH	703MC14017BP	MC14017BCP	04713
U33	IC CMOS DEC CNTR 5STAGE JOH	703MC140176P	MC14017BCP	04713

ASSEMBLY OPTION (D15) // BCD OUTPUT
ASSEMBLY NUMBER 12807955-1
REFERENCE DESIGNATOR PREFIX 1A3A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
	***** ADD *****			
U40	IC CMOS HEX BUFFER	703MC14050BP	MC14050BCP	04713
U41	IC CMOS HEX BUFFER	703MC14050BP	MC14050BCP	04713
U42	IC CMOS HEX BUFFER	703MC14050BP	MC14050BCP	04713
U43	IC CMOS HEX BUFFER	703MC14050BP	MC14050BCP	04713
U44	IC CMOS HEX BUFFER	703MC14050BP	MC14050BCP	04713

6.2.4. Milliseconds Output (Option E14) (Schematic Dwg. No. 12308192-02)

General Description

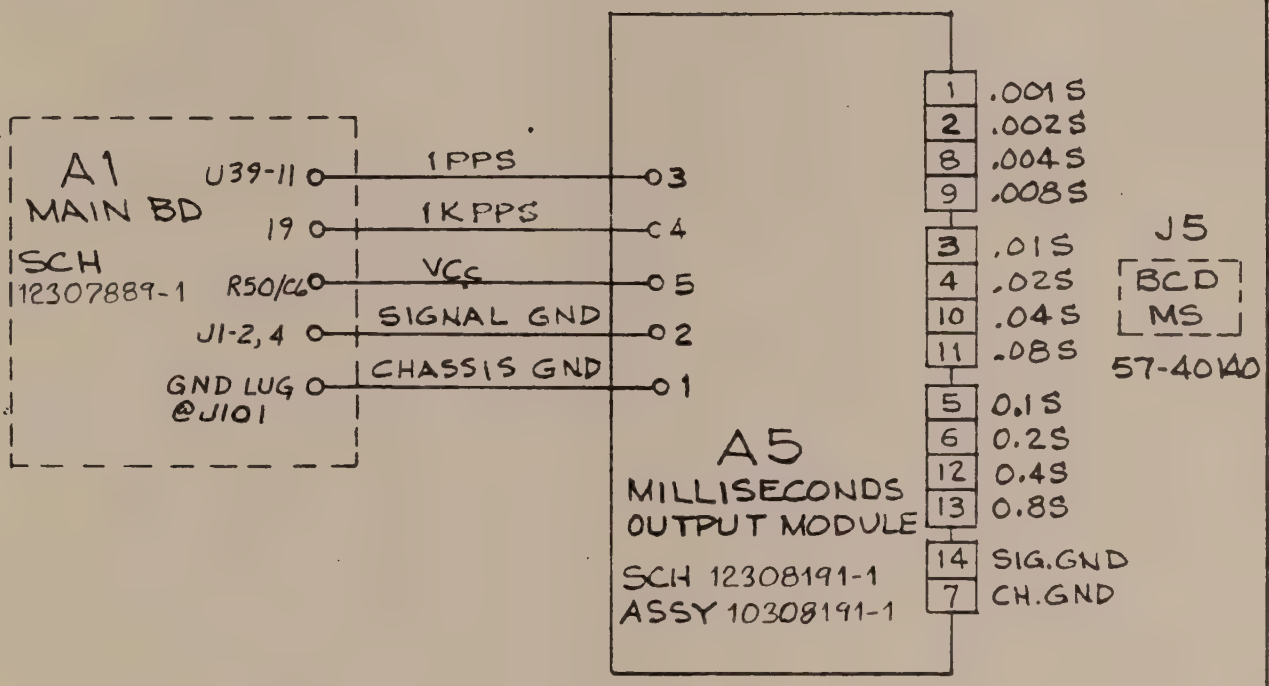
Option E14 adds parallel BCD Milliseconds outputs to the Model 8730 Time Code Reader. Milliseconds Output Module A5 with rear panel connector J5 and associated wiring is added to the basic unit.

Specifications

Three digits (twelve bits) of parallel BCD milliseconds are provided as outputs.

Code:	8-4-2-1
Logic:	ONE = 2.4 to 3.2 V at 200 uA
	ZERO = 0 to 0.4 V, 3.6 mA sink

REVISIONS					
LTR	DESCRIPTION	ENG. NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS			7/9	KH
B	DWG NO. WAS 08119202		4837		
C	AUSTRON RELEASE		—	11/85	OK



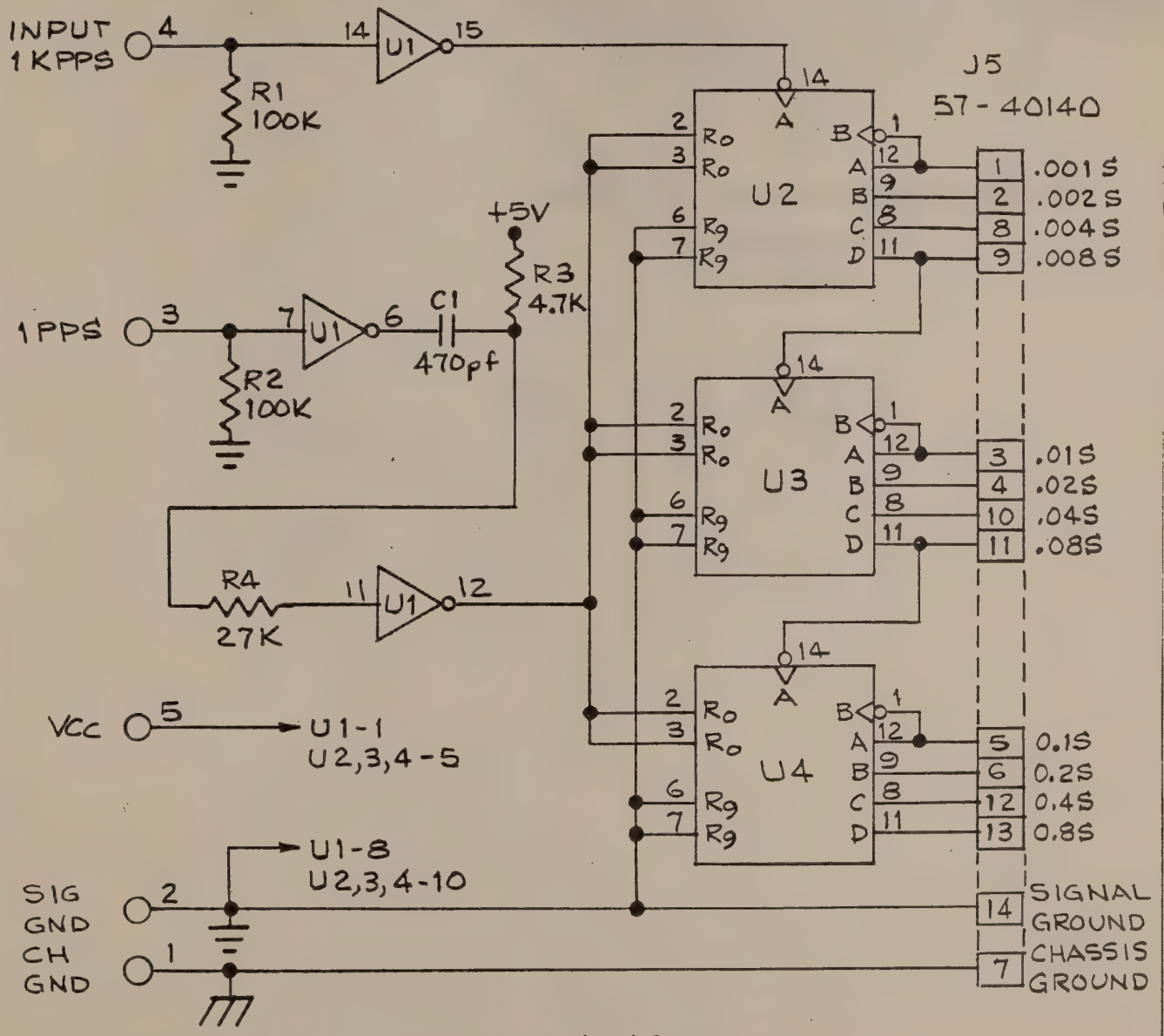
CIRCUITRY SHOWN TO BE SUPERIMPOSED ON THE BASIC BLOCK DIAGRAM 12407900-1

		DRAWN 8/30/79 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.01 .XXX ±.001 ANGLES ±	AUSTRON INC. AUSTIN, TEXAS	MILLISECONDS OUTPUT OPTION E14
		CHECK DATE			
		ELECT. DATE			
		MECH. DATE			
		PROJECT DATE		CODE IDENT 24672	
8730 - E14		Q.A. DATE		MATERIAL	DWG NO 12308192-2 C
USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING	DWG SIZE A	
APPLICATION				SH 1 OF 1	

ASSEMBLY MILLISECONDS OUTPUT E14 OP1
ASSEMBLY NUMBER 12808192-3
REFERENCE DESIGNATOR PREFIX 1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
	***** ADD *****			
A3A5	PCB ASSY, MILLISECONDS MODULE	10308191-1		24672
	** SHIP WITH **			
P5	CONN 14 PIN PLUG	551306-0000	57-30140	02660

REVISIONS					
ITEM	DESCRIPTION	SUB. NO.	ECO NO.	DATE	APP. BY
A	RELEASE TO RECORDS			10/79	KH
A1	ADDED PINS 11 & 12 TO U1		NFC	10/79	[illegible]
A2	R3 WAS 56K. (ECR 132-79)	-	NFC	11/20/79	
B	DWG NO. WAS 08119101		4837		
C	REVISED PER ECO 6804		6804	10-24-84	OK

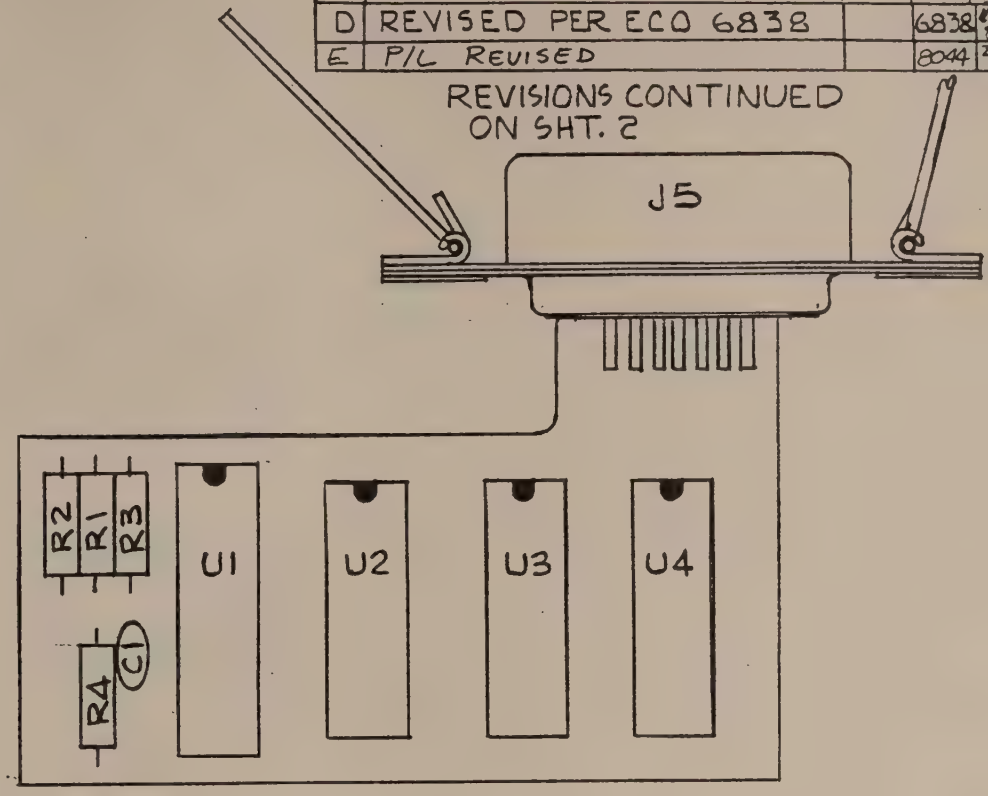


U1 = CD4049AE
U2, U3 & U4 = SN74HC90N

		DRAWN DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	AUSTRON INC. AUSTIN, TEXAS	MILLISECONDS OUTPUT	
		CHECK DATE				
		ELECT. DATE				
		MECH. DATE				
8730		PROJECT DATE 10/79		CODE IDENT. 24672		
8720		Q.A. DATE		MATERIAL	REF 7	DWG NO. 12308191-1 ISSUE C
USED ON	NEXT ASSY	SCALE —	DO NOT SCALE DRAWING	DWG SIZE A	SH 1 OF 1	
APPLICATION						

REVISIONS					
ISSUE	DESCRIPTION	SHT. NO.	ECO NO.	DATE	APP. BY
A	RELEASE TO RECORDS	—		10/29/79	KH
A1	SHT. 2 : R3 (4.7K) WAS 56K • (ECR 172-79)		NEC	12/17/79	
B	DWG NO. WAS 08119101		A837		
C	REVISED PER ECO 6804		6804	10-24-84	DL
D	REVISED PER ECO 6838		6838	6-7-85	DL
E	P/L REVISED		8044	2/4/86	DL

REVISIONS CONTINUED ON SHT. 2



		DRAWN Ebert 7/ DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±, .XX ±, .XXX ±, ANGLES ±	AUSTRON INC. AUSTIN, TEXAS	P.C. ASSY MILLISECONDS MODULE
		CHECK DATE			
		ELECT. DATE			
		MECH. DATE			
8730	E14	PROJECT DATE		CODE IDENT. 27672	
8720	E14	Q.A. DATE		MATERIAL	REF
USED ON	NEXT ASSY	SCALE 2:1	DO NOT SCALE DRAWING	DWG SIZE A	DWG NO. 10308191-1 REV F
APPLICATION				SH 1 OF 2	

ASSEMBLY PCB ASSY, MILLISECONDS MODULE
ASSEMBLY NUMBER 10308191-1
REFERENCE DESIGNATOR PREFIX 1A3A5
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	CAP CERA RDL COG 470 PF 100V 5%	601110-0471	CN20A471J242	71590
J5	CONN 14 PIN SOCKET CHASSIS RCPT	551306-0005	57-40140	02660
R1	RES FXD COMP 100 K 1/4W 05%	651100-0104	RC07GF104J	81349
R2	RES FXD COMP 100 K 1/4W 05%	651100-0104	RC07GF104J	81349
R3	RES FXD COMP 4.7 K 1/4W 05%	651100-0472	RC07GF472J	81349
R4	RES FXD COMP 27 K 1/4W 05%	651100-0273	RC07GF273J	81349
U1	IC CMOS HEX INV/BUFF	703MC14049BP	MC14049UBCP	04713
U2	IC HSCMOS DECADE COUNTER	70374HC90N	MC74HC90N	04713
U3	IC HSCMOS DECADE COUNTER	70374HC90N	MC74HC90N	04713
U4	IC HSCMOS DECADE COUNTER	70374HC90N	MC74HC90N	04713

7. SPECIAL MODIFICATIONS

7.1. SCOPE OF SECTION

Section Seven provides circuit descriptions, logic and schematic diagrams, assembly drawings, and parts lists for special or non-standard options included in your Model 8730.

7.2. MODIFICATIONS INCLUDED

Modifications to the Model 8730, requested by the customer, are documented in this section. These are usually extra-cost items to tailor the unit for a specific application.

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